

Site-Controlled Uniform Ge/Si Hut Wires with Electrically Tunable Spin–Orbit Coupling

Fei Gao, Jian-Huan Wang, Hannes Watzinger, Hao Hu, Marko J. Rančić, Jie-Yin Zhang, Ting Wang, Yuan Yao, Gui-Lei Wang, Josip Kukučka, Lada Vukušić, Christoph Kloeffel, Daniel Loss, Feng Liu, Georgios Katsaros,* and Jian-Jun Zhang*

Semiconductor nanowires have been playing a crucial role in the development of nanoscale devices for the realization of spin qubits, Majorana fermions, single photon emitters, nanoprocessors, etc. The monolithic growth of site-controlled nanowires is a prerequisite toward the next generation of devices that will require addressability and scalability. Here, combining top-down nanofabrication and bottom-up self-assembly, the growth of Ge wires on prepatterned Si (001) substrates with controllable position, distance, length, and structure is reported. This is achieved by a novel growth process that uses a SiGe strain-relaxation template and can be potentially generalized to other material combinations. Transport measurements show an electrically tunable spin–orbit coupling, with a spin–orbit length similar to that of III–V materials. Also, charge sensing between quantum dots in closely spaced wires is observed, which underlines their potential for the realization of advanced quantum devices. The reported results open a path toward scalable qubit devices using nanowires on silicon.

Semiconductor nanowire (NW) devices have become the workhorse for studying exotic states such as Majorana fermions,^[1,2] Andreev bound states,^[3,4] for realizing spin qubits,^[5,6] programmable NW circuits,^[7] nanolasers,^[8] and solar cells.^[9] Different material combinations ranging from II–VI to IV–IV have been widely used. Among them, Ge is attracting more and more

attention due to its high hole mobility,^[10–13] low effective mass in 2D hole gases,^[14,15] good contacts with metals,^[16–18] strong spin–orbit interactions,^[19–22] capability of isotopic purification,^[23] and compatibility with Si. These attractive features make Ge a promising candidate not only as a transistor channel material but also as a host for spin^[6,24,25] and even topological qubits.^[26,27] Excitingly, the first hole spin qubit^[6] and proximity-induced superconductivity with a hard gap^[28] have been realized recently in 1D Ge.

Despite much progress that has been made so far, it remains a formidable challenge to have individuals as well as arrays of NWs with a high degree of addressability and scalability for the next generation of NW-based quantum devices. For example, in the field of group III–V

semiconductors, precisely positioned NW networks have been achieved with predefined metal islands.^[29] The out-of-plane grown NW structures, however, need to be transferred from the growth wafer to a second substrate for device fabrication, which limits their scalability.^[7,29] Very recently, high-quality in-plane NW networks have been successfully demonstrated with

Dr. F. Gao, J.-H. Wang, J.-Y. Zhang, Prof. T. Wang, Prof. Y. Yao, Prof. J.-J. Zhang
National Laboratory for Condensed Matter Physics and Institute of Physics
Chinese Academy of Sciences
100190 Beijing, China
E-mail: jjzhang@iphy.ac.cn

Dr. F. Gao, J.-H. Wang, J.-Y. Zhang, Prof. T. Wang, Prof. J.-J. Zhang
CAS Center for Excellence in Topological Quantum Computation and School of Physics
University of Chinese Academy of Sciences
100049 Beijing, China

 The ORCID identification number(s) for the author(s) of this article can be found under <https://doi.org/10.1002/adma.201906523>.

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^[†]Present address: Total@Saclay, Nano-INNOV-Bât. 861, 8 Boulevard Thomas Gobert, 91120 Palaiseau, France

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Dr. H. Watzinger, J. Kukučka, Dr. L. Vukušić, Prof. G. Katsaros
Institute of Science and Technology Austria
Am Campus 1, 3400 Klosterneuburg, Austria
E-mail: georgios.katsaros@ist.ac.at

Prof. H. Hu
Frontier Institute of Science and Technology
Xi'an Jiaotong University
710054 Xi'an, China

Dr. M. J. Rančić,^[†] Dr. C. Kloeffel, Prof. D. Loss
Department of Physics
University of Basel
Klingelbergstrasse 82, CH-4056 Basel, Switzerland

Prof. G.-L. Wang
Institute of Microelectronics
Chinese Academy of Sciences
100029 Beijing, China

Prof. F. Liu
Department of Materials Science and Engineering
University of Utah
Salt Lake City, 84112 UT, USA

Prof. T. Wang, Prof. J.-J. Zhang
Songshan Lake Materials Laboratory
523808 Dongguan, Guangdong, China

selective-area^[30,31] and template-assisted^[32] growth techniques, but the problems related to growth imperfections such as dislocation and polytypism still remain. In addition, the selective-area growth works only for material systems that have good growth selectivity between oxides and semiconductors. In the field of group IV Si/Ge system, attempts have been made on rib-patterned Si (1 1 10) substrate and positioned in-plane Ge wire bundles have been demonstrated.^[33] However, isolated wires could not be obtained, which is a prerequisite for scalable quantum devices.

Here, combining bottom-up self-assembly and top-down nanofabrication, we demonstrate the self-controlled growth of highly uniform in-plane Ge wires on Si (001) substrates, which are both addressable and scalable. The so-called Ge hut wires (HWs)^[34] grow selectively on an initially formed 1D SiGe layer at the edges of trench-patterned Si. They have a height of about 3.8 nm with a standard deviation of merely 0.11 nm, and their position, distance, length, and structure can all be precisely controlled to exhibit an unprecedented high degree of uniformity. Theoretical calculations show that the initially grown 1D SiGe layer provides an enhanced strain relaxation and results in the formation of the Ge HW. Low temperature co-tunneling measurements were performed to determine the spin-orbit coupling (SOC) strength of the Ge HWs. A theoretical model has been developed to extract the SOC length from the experimentally measured singlet-triplet anticrossing, which concludes that the SOC length of holes in the Ge HWs is comparable to that of electrons in InAs and InSb. Transport measurements further reveal that the SOC length is electrically tunable. In addition, the formation of two closely spaced parallel Ge HWs enables capacitive coupling and thus charge sensing between quantum dot (QD) devices.

In order to obtain site-controlled Ge wires, ordered trenches are fabricated by electron-beam lithography and reactive ion etching on an 8 in. Si (001) wafer, as shown by the atomic force microscope (AFM) image in **Figure 1a**. The patterned wafer is cut into $10 \times 10 \text{ mm}^2$ or $16 \times 16 \text{ mm}^2$ pieces to fit sample adaptors for molecular beam epitaxy (MBE) growth. These trenches with an 80 nm width and a 70 nm depth have steep sidewalls with inclination angle above 65° and are oriented along either the [100] or the [010] direction (see the Experimental Section for a description of the cleaning procedure and the growth details). After the deposition of a 60 nm Si buffer layer and a 3 nm $\text{Si}_{0.75}\text{Ge}_{0.25}$ alloy at 550 °C, uniform 1D SiGe structures with a trapezoidal cross-section (called from now on mounds) form at the two edges of the trenches as shown in **Figure 1b**. After the subsequent deposition of 0.6 nm Ge at 550 °C followed by 1 h in situ annealing, Ge wires form on the SiGe mounds (**Figure 1c**). The initial formation of the 1D SiGe mound is found a prerequisite for the subsequent growth of the Ge HW. The Ge HWs have two (105) facets with an inclination angle of 11.3° , as shown by the surface orientation map in the inset of **Figure 1c**. This is further confirmed by the cross-sectional scanning transmission electron microscopy (STEM), showing the (105)-faceted cross-section with a height of about 3.8 nm (**Figure 1d**). Interestingly, as shown in the inset of **Figure 1d**, the SiGe mound shows an asymmetric trapezoidal geometry (the cross-section is schematically shown in **Figure 3a**). A sharp interface between the Ge wire and the SiGe mound is observed. No dislocations are observed both

in cross-section and along the wire (**Figure 1d–g**), indicating a perfect single crystal growth of the wires. The height distribution of the Ge HWs is shown in **Figure 1h**. There is an average height of 3.8 nm and a standard deviation of 0.11 nm. The morphological evolution during the growth is summarized in **Figure 1i**.

As shown above, the wires form at the edges of the trenches, which are fully controllable by the top-down fabrication. We are therefore able to grow HWs with controlled position, distance, length, and even structure on a wafer scale. By simply changing the top width of the ridges, the areas between the trenches, we can create two parallel Ge HWs with a neighboring edge-to-edge distance of about 30 nm (**Figure 2a**). This distance is tunable and can be further decreased. However, due to strain repulsion,^[35] neighboring wires do not merge together into one wire. The length of the HWs depends only on the length of the trenches, which implies that in principle any length can be obtained. For example, by changing the trench length from 4 to 10 μm , we correspondingly obtained ordered Ge HWs with a length of 10 μm (**Figure 2b**). It is apparent that one can tune the wire period and distance by choosing a different pattern period, as shown in **Figure 1a,b**. Particular geometries like square-shaped structures consisting of four HWs (**Figure 2c**) and L-shaped structures consisting of two perpendicular HWs (**Figure 2d**) can also be obtained. For the inner squares (**Figure 2c**), the wires are connected and form a closed loop, while, for the outer squares, they are mostly disconnected. We expect that connected outer squares can be obtained by tuning the pattern period or the trench sidewall slope. At the ends of the T-shaped trench structure (**Figure 2d**), one sees larger Ge islands. Their growth is attributed to a larger capture zone of these positions where there are more Ge ad-atoms to diffuse into, resulting in large islands.^[36] It could be avoided by decreasing the pattern period. We emphasize that all the HWs are homogeneous with a stable lateral size, not depending on the pattern period, length, and structure.

Let us now elaborate on the growth mechanism of the site-controlled Ge wires. When the strained SiGe alloy is deposited on the Si substrate, it first wets the surface of both the flat region and the deep trench. The trench with steep sidewall induces notable strain relaxation at the rim, which directs the further deposited SiGe to accumulate at the rim to form a SiGe mound, as observed for the preferential growth of SiGe islands at edges of pits with steep sidewall.^[37] The SiGe mound is seen to have a base size of $\approx 70 \text{ nm}$, which is well below the minimum size required to form the faceted SiGe wire,^[34] and hence adopts a shape with continuous changing surface orientation and zero contact angle with the flat region.^[38] On the other hand, upon SiGe deposition, the upper sidewall of the trench evolves into a shallow (105) facet, which continues into the sidewall of the SiGe mound. Consequently, the SiGe mound adopts an asymmetric shape with the (105) faceted sidewall next to the trench and a shallower sidewall on the other side.

Next, we explain why the Ge HWs form preferably on the SiGe mounds. In general, the growth of strained nanostructures, such as nanoislands, wires, or more complex structures, is governed by the competition between surface energy and strain relaxation energy.^[39–41] Here, we develop a quantitative

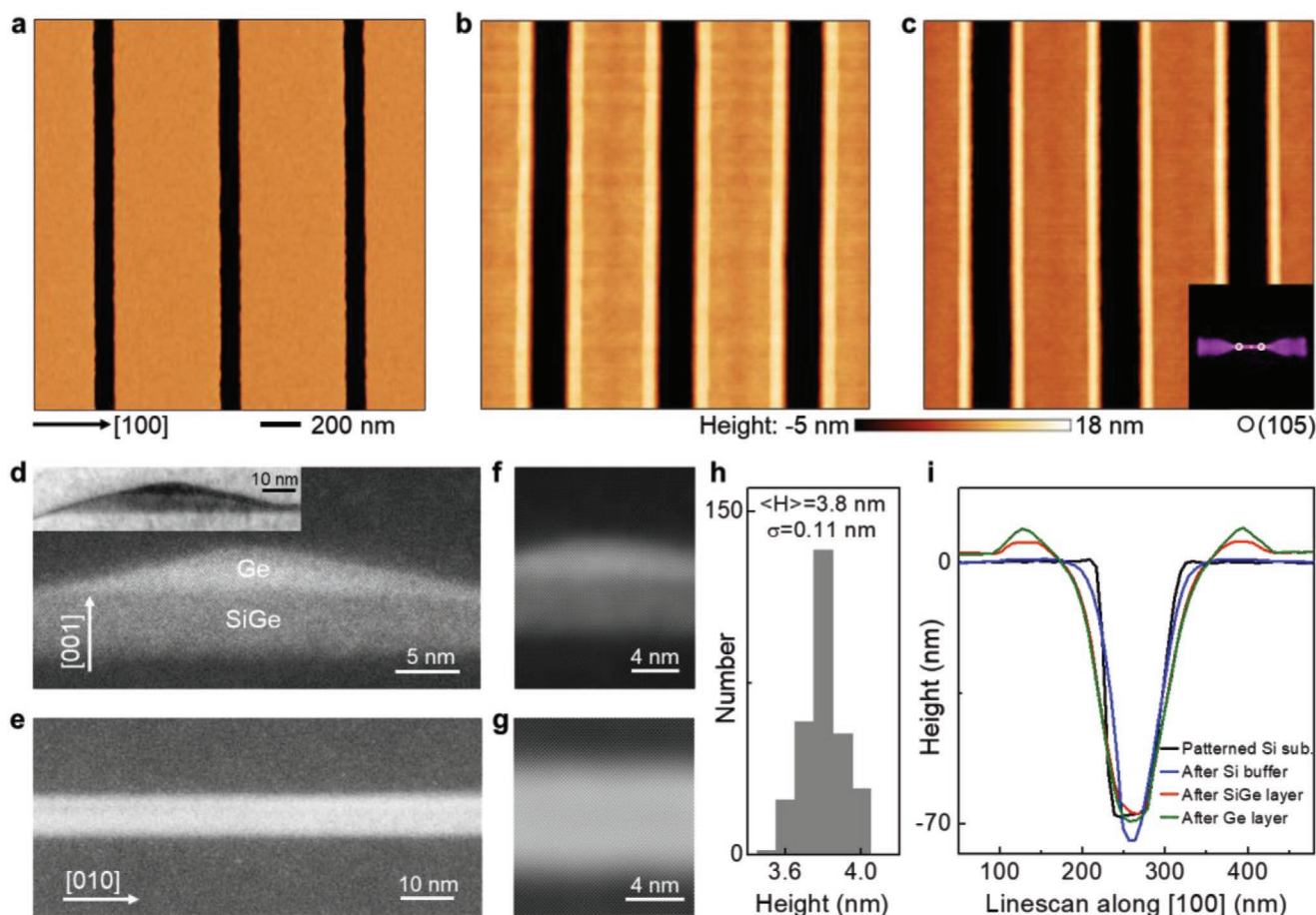


Figure 1. Self-assembled growth of site-controlled Ge HWs at the edges of a trench-patterned Si (001) substrate. a–c) AFM images of: a) a [010] oriented trench-patterned Si(001) substrate, b) $\text{Si}_{0.75}\text{Ge}_{0.25}$ mound structures formed at the two edges of the trenches, and c) Ge HWs grown on the $\text{Si}_{0.75}\text{Ge}_{0.25}$ mound. The black areas in all images are the etched trenches, while the bright 1D structures correspond to the SiGe mounds in (b) and the Ge wires in (c). The inset in (c) shows a surface orientation map demonstrating that the wires are (105) faceted with an inclination angle of 11.3° . d,e) STEM images of a wire in cross-section and along the wire, respectively. The cross-section shows the triangular Ge HW sitting on the SiGe mound. As seen from the inset TEM image in (d) and the red AFM linescan in (i), the SiGe mounds have an asymmetric trapezoidal cross-section. The side next to the trench has a slope of 11.3° , while the side away from the trench has a slope of about 9° . f,g) Filtered STEM images with higher resolution for a wire in cross-section and along the wire, respectively. h) Histogram showing the height distribution of the Ge HWs. The average height value $\langle H \rangle$ and standard deviation σ of the distribution are quoted. The Ge HW height is extracted by the measured AFM peak height (green curve in (i)), with the addition of the wetting layer thickness and the subtraction of the $\text{Si}_{0.75}\text{Ge}_{0.25}$ mound thickness (red curve in (g)). i) AFM linescans along the [100] direction over one trench showing the evolution of the substrate from before growth (black), after Si buffer (blue) and SiGe layer growth (red) until the final formation of the two site-controlled Ge HWs (green). The 60 nm height offset of the buffer layer has been subtracted from the black trace.

theoretical model to show that it is the enhanced strain relaxation that drives the Ge HW to grow on a pregrown SiGe mound, rather than on a flat surface (Figure 3a,b). We analyze the free energy difference (dE) between a Ge HW grown on the SiGe mound and a Ge HW grown on a flat surface. If $dE < 0$, the Ge wire is preferred to grow on the SiGe mound; if $dE > 0$, on the flat surface.

Figure 3b shows the free energy difference as a function of inclination angle (α) and height (h) of the SiGe mound. (The detailed model and derivation are described in the Supporting Information.) One can see that for large enough α , dE is negative, meaning that the Ge wire growth on the SiGe mound is energetically favorable; while for relatively small α , dE is positive and the Ge wire prefers to grow on a flat surface. The boundary between the two regions can be determined by letting

$dE = 0$, which gives the boundary line h_m as a function of α , as shown by the black curve in Figure 3b. The general trend predicted by the model agrees very well with the experiments.

Furthermore, it has been shown that the diffusion barriers of Si and Ge ad-atoms on Si and Ge(001) surfaces increase with increasing compressive strain.^[42,43] For pure Ge HW growth (without SiGe mound), the misfit strain of the wetting layer is high, so that the diffusion barrier is larger, favoring the formation of nanoislands. In contrast, by growing the SiGe alloy first, the diffusion barrier is reduced because of a smaller misfit strain, favoring the growth of the very long SiGe mounds. Later, when pure Ge is grown, the SiGe mounds act as a “diffusion buffer,” so that the diffusion barrier of Ge ad-atom is smaller on the mounds than on the flat surface, which again favors the growth of long Ge HWs.

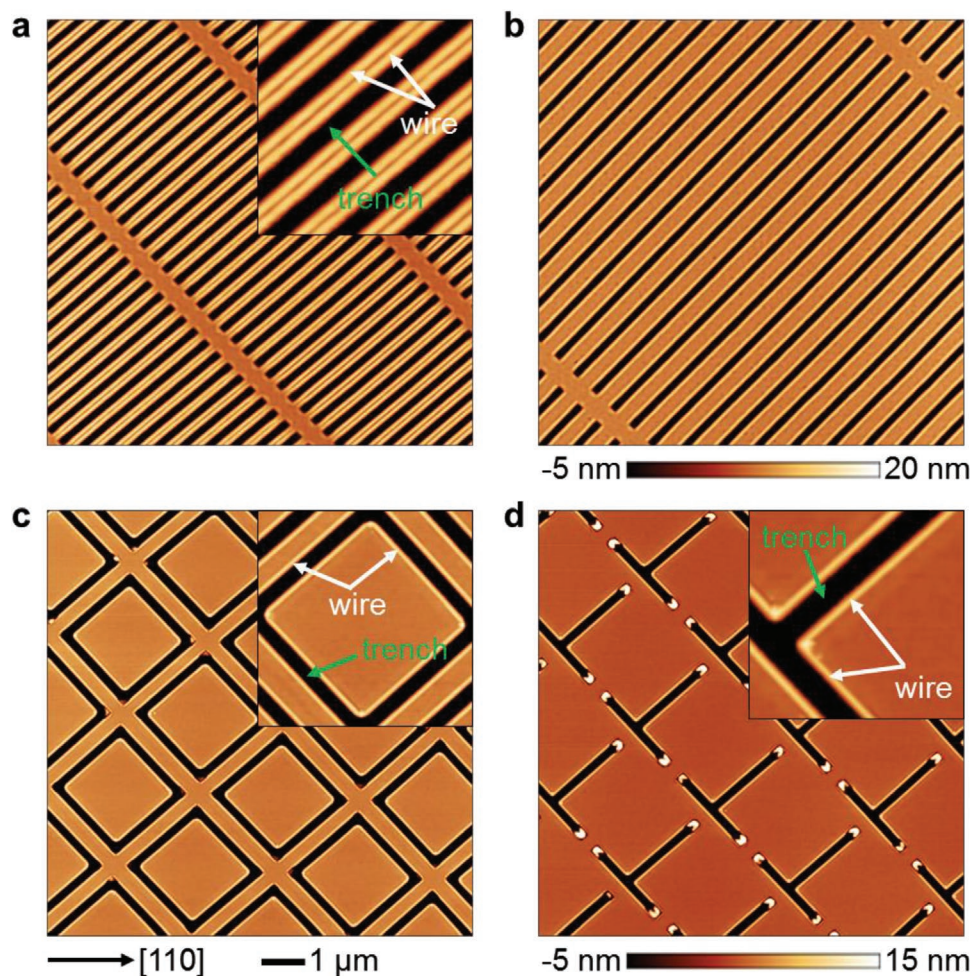


Figure 2. Site-controlled Ge HWs with controllable period, length, and structure. a) AFM image of parallel HWs grown on a Si substrate with trenches of 4 μm in length and periodicity of 400 nm. The inset shows a zoom-in of the closely spaced parallel Ge HWs separated by about 30 nm. (b) is similar to (a) but for trenches with a period of 600 nm and a length of 10 μm . c) AFM image of Ge HWs grown on a Si substrate with trenches forming a square shape. The inset shows square-shaped HW structures consisting of four HWs. d) AFM image of Ge HWs grown on a Si substrate with T-like trenches. L-shaped structures consisting of two perpendicular Ge HWs are created. In all images, the wires are oriented along the [100] or [010] direction.

A key parameter for NWs, both in view of their potential to host Majorana bound states and hole spin qubits is the SOC strength. In order to investigate this important parameter in our system, single hole transistors (Figure 4a) were fabricated out of the site-controlled HWs (see the Experimental Section for details), and low temperature magnetotransport measurements were performed. Differential conductance (dI/dV) was measured as a function of the source–drain bias (V_{SD}) and the gate voltage (V_G). These measurements verified the realization of single hole transistors as closing Coulomb diamonds can be observed in Figure 4b. Elastic co-tunneling and inelastic co-tunneling features (indicated by dashed yellow lines in Figure 4b),^[45] leading to finite conductance within the Coulomb diamonds, is present due to the good electrical contacts to the HWs. In inelastic co-tunneling the transition between the ground state and excited states can be observed and thus be used for performing spectroscopy measurements. For a diamond with an odd hole occupation number and for a fixed gate voltage value within the Coulomb blockade regime, the transition between the spin ground and excited state can

be seen when sweeping the magnetic field. This allows the measurement of the Zeeman splitting and thus the extraction of the g -factors (Figure 4c,d) and their anisotropy (Figure 4e). Furthermore, by changing the number of confined holes by one, an even hole occupancy is achieved. The numerical derivative d^2I/dV^2 as a function of V_{SD} and B_{\parallel} (Figure 4f) shows that the excited state comprises three states, with all three splitting nonlinearly in the magnetic field. We account this nonlinearity in the Zeeman splitting to orbital effects. By changing the direction of the magnetic field, from in-plane (B_{\parallel}) to out-of-plane (B_{\perp}) direction where the g -factor is a factor of 8 larger, a ST_{\perp} anticrossing can be observed around $B_{\perp} = 1$ T (Figure 4g–i). Due to the fact that the g -factor is much larger for the B_{\perp} direction, we are able to identify the anticrossing before any orbital effects start to be significant. Such an anticrossing indicates the presence of SOC in the site-controlled Ge HWs with an anticrossing ($\Delta_{ST_{\perp}}$) of about 35 μeV .

Attention is now turned to a second device for which data at the low and even hole number regime was obtained. We investigate the effect of the applied electric field on the SOC strength.

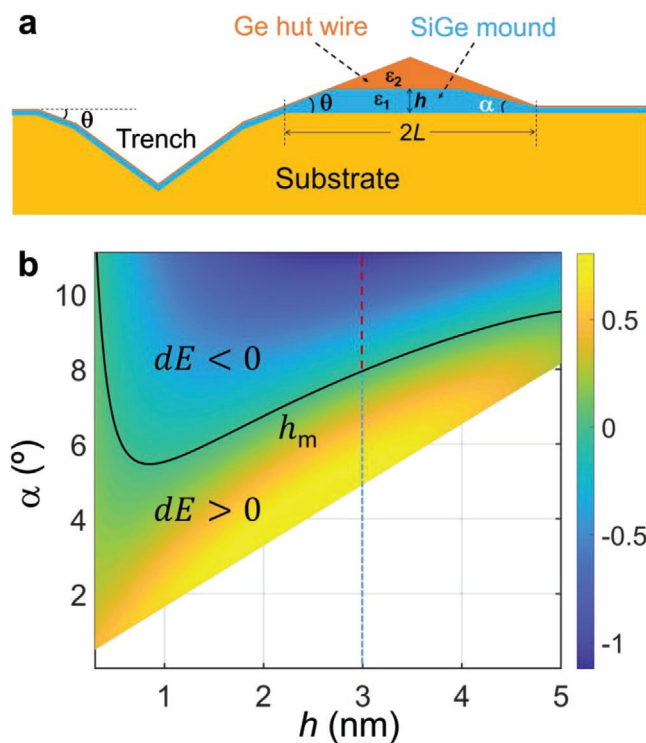


Figure 3. Free energy difference between a Ge HW grown on a $\text{Si}_{0.75}\text{Ge}_{0.25}$ mound and that on a flat Si with the same volume. a) Schematic model for the Ge HW growth on a pregrown SiGe mound. $2L$ is the base size of the pregrown SiGe mound and h is its height. α is the inclination angle of the SiGe mound at the edge away from the trench and θ is the inclination angle of the SiGe mound at the edge next to the trench and the facet angle of the Ge HW. ϵ_1 and ϵ_2 are respectively the mismatch strain of the SiGe mound and the Ge HW with respect to the substrate Si. b) Free energy difference dE , in units of eV, versus mound inclination angle α and height h . The black line h_m indicates the boundary between positive and negative dE . The dotted line corresponds to the experimental value of the SiGe mound height. $\epsilon_1/\epsilon_2 = 0.25$ is used in the calculation, in accordance with the Ge concentration in the $\text{Si}_{0.75}\text{Ge}_{0.25}$ alloy.

Figure 5a,b shows the dI/dV versus V_{SD} and B_{\perp} for increasing gate voltage value. It can be clearly observed that the magnitude of the anticrossing increases with the applied top gate voltage. We model the electric field dependence of the spin–orbit coupling with the following Hamiltonian

$$H_{SO} = \alpha' k_y \sigma_x \quad (1)$$

where k_y is the momentum (wavenumber) along the HW and σ_x is the x -component of the spin operator. The partly phenomenological spin–orbit coupling coefficient $\alpha' = (\alpha_{DR} + \alpha)E_z + \beta$ is composed of the part $(\alpha_{DR} + \alpha)E_z$ that depends on the electric field E_z and the part β that is independent of the electric field. To elaborate more, α_{DR} is the direct Rashba coefficient, which is a function of the dimensions of the wire, material parameters, and strain parameters (see Section IV in the Supporting Information); α and β are phenomenological parameters that depend, e.g., on the microscopic details of the interfaces.

Our method of calculating the ST_{-} anticrossing is based on the approach of ref. [46], adapted for a 1D problem. We start by obtaining an analytical expression for singlet and triplet wave

functions of two charged particles in a harmonic oscillator potential, valid in the limit of strong Coulomb repulsion (for more information, see Sections V and VI in the Supporting Information). The $\Delta_{ST_{-}}$ anticrossing is given by

$$\Delta_{ST_{-}} = 3^{1/4} \sqrt{2} \frac{|\alpha'|}{\lambda_c} \quad (2)$$

where λ_c is the confinement length of the quantum dot. The relation between λ_c , the orbital level spacing $\hbar\omega$, and the effective mass m^* is $\lambda_c = \sqrt{\hbar/(m^*\omega)}$. Furthermore, the orbital level spacing is related to the ST_0 splitting Δ_{ST_0} through the formula $\Delta_{ST_0} = \hbar\omega\sqrt{3}$ (see Section VI in the Supporting Information, where Δ_{ST_0} corresponds to ΔE_{ST}). The ST_0 splitting Δ_{ST_0} can be read out from Figure 5a,b, thus allowing us to also obtain the orbital level spacing $\hbar\omega$, while the effective mass m^* is an unknown parameter due to the unknown number of holes confined in the quantum dot. Although the effective mass is an unknown parameter it is reasonable to assume that the effective mass is between the light hole and the heavy hole effective masses in germanium, i.e., $m_{LH} \leq m^* \leq m_{HH}$, with $m_{LH} = 0.042m$ and $m_{HH} = 0.32m$, where m is the free electron mass. After obtaining the value of α' from the magnitude of the anticrossing $\Delta_{ST_{-}}$, the SOC length is calculated as $\lambda_{SO} = \hbar^2/(m^*|\alpha'|)$ and these results are displayed in Figure 5c,d. As explained in Section VIII in the Supporting Information, this result is consistent with previous studies.^[47,48]

For $m_{LH} \leq m^* \leq m_{HH}$, we obtain $600 \text{ nm} \geq \lambda_{SO} \geq 200 \text{ nm}$ for the maximum achievable value of the electric field $E_z = -5 \text{ V } \mu\text{m}^{-1}$. The spin–orbit length is comparable to values expected in InAs and InSb, where the spin–orbit length is $\approx 200 \text{ nm}$.^[48–50] The spin–orbit strength has such a large value although the electric field used in the experiment is not optimized. Further increases in the spin–orbit strength can be engineered by varying the electric field over a larger range of values. Our findings show that $1.9 \times 10^{-11} \text{ eV m} \geq (\alpha_{DR} + \alpha)E_z \geq 6.05 \times 10^{-12} \text{ eV m}$ at $E_z = -5 \text{ V } \mu\text{m}^{-1}$ and $-1.6 \times 10^{-11} \text{ eV m} \leq \beta \leq -4.7 \times 10^{-12} \text{ eV m}$ indicating an interplay between electric-field-dependent and electric-field-independent SOC mechanisms. For more details on SOC, we refer the reader to Sections IV and VI in the Supporting Information.

We next focus on the potential of the site-controlled Ge wires for the realization of scalable quantum devices. For this, we investigate the capacitive coupling between single QDs formed in parallel wires (Figure 2a), because such a capacitive coupling is important for charge sensing applications. Devices out of two single QDs facing each other have been fabricated (Figure 6a). When sweeping the two gate voltages V_{G1} and V_{G2} of gates G1 and G2 versus each other and measuring the sum of the currents through both QDs in devices 1 and 2, a typical stability diagram of a parallel double QD is obtained (Figure 6b). At the intersectional points of the Coulomb peaks, shifts, demonstrating charge sensing, can be observed caused by single hole tunneling events in each of the two devices. A zoom-in to the Coulomb oscillations of device 1 (2) is shown in the left (right) panel of Figure 6c. Dashed white lines indicate the positions of the characteristic breaks of the lines. The shifts correspond to about $0.02e$ and $0.13e$ for devices 1 and 2, respectively, where e

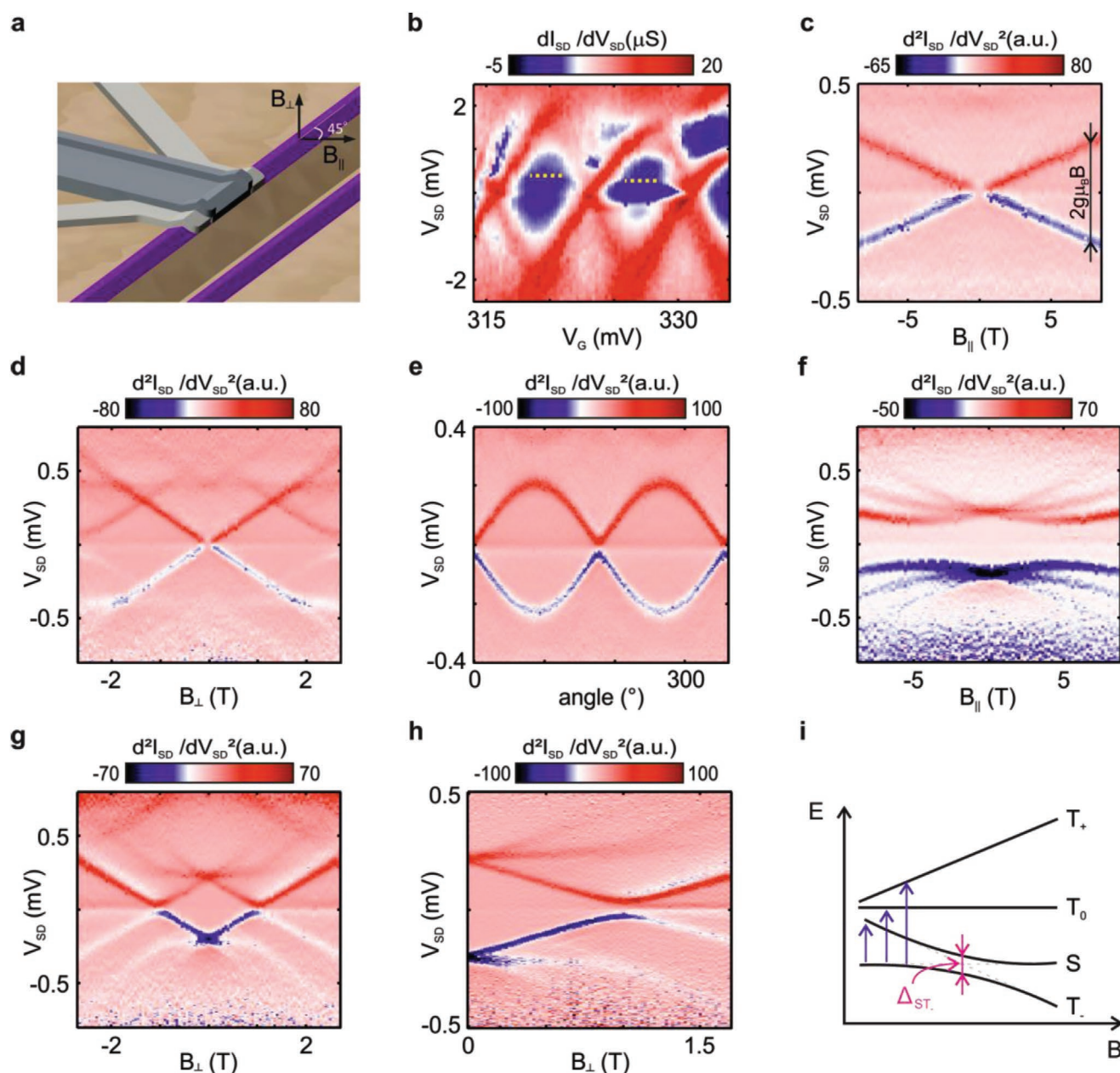


Figure 4. Magnetotransport measurements of single QD devices and singlet–triplet anticrossing. a) Schematic of a three terminal site-controlled HW device. Light gray electrodes indicate source and drain contacts while the darker gray electrode is the top gate. The insulator is not shown. b) dI/dV versus V_{SD} and V_G at zero magnetic field showing the characteristic diamond plot. Inside the Coulomb diamonds, elastic co-tunneling and inelastic co-tunneling steps (marked by yellow dashed lines) can be observed. c,d) d^2I/dV^2 versus V_{SD} and parallel (perpendicular) magnetic field $B_{||}$ (B_{\perp}) for $V_G = 320.9$ mV. The Zeeman splitting of the ground state with an odd hole number can be clearly observed. g -factors of 0.50 ± 0.01 and 3.91 ± 0.02 can be extracted for $B_{||}$ and B_{\perp} , respectively. e) d^2I/dV^2 versus V_{SD} and angle of magnetic field for $B = 1$ T and $V_G = 320.9$ mV. A g -factor anisotropy of about 8, underlying the heavy-hole character of the confined states,^[44] is measured. Zero degrees correspond to the parallel magnetic field direction $B_{||}$ and 90° to the out-of-plane field B_{\perp} . f,g) d^2I/dV^2 versus V_{SD} and $B_{||}$ (B_{\perp}) for $V_G = 327.9$ mV and an even hole QD occupation. h) High-resolution measurement similar to (g) for highlighting the singlet–triplet anticrossing at about 1 T. At the anticrossing, the T-state becomes the ground state. i) Energy diagram showing the threefold splitting of the triplet state with magnetic field. Due to spin–orbit coupling, the lowest energy triplet and the spin-singlet state anticross.

is the electron charge. The difference in the shift is due to the different leverarm factor of the two QD gates.^[51]

In summary, in this study, we developed a method for monolithic growth of site-controlled Ge wires without the use of any metal catalyst. The method relies merely on strain relaxation

via a pregrown SiGe structure. Such a strain energy relaxation mechanism of a system having a large lattice mismatch via an intermediate layer having a smaller lattice mismatch is general. It is therefore applicable to similar materials including III–V nanowires, which are foremost candidates for topological

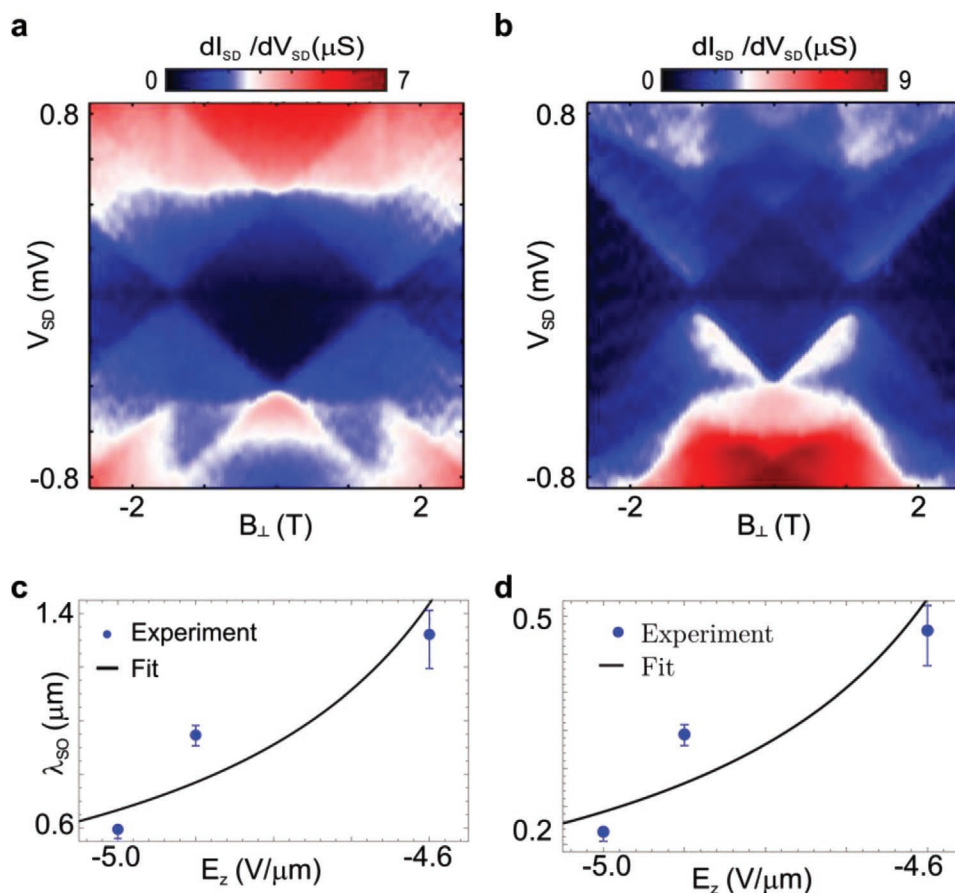


Figure 5. Electrical tunability of spin-orbit coupling. a, b) dI_{SD}/dV_{SD} versus V_{SD} and B_{\perp} for $V_G = 510.5$ and 550 mV, respectively. Δ_{ST} increases from 29 to 63 μeV , occurring at magnetic field strength of 1–2 T. c, d) Spin-orbit length versus the vertical electric field strength for c) a light-hole and d) a heavy-hole effective mass. The fitted parameters are $-3.8 \times 10^{-18} e m^2 \leq \alpha_{DR} + \alpha \leq -1.21 \times 10^{-18} e m^2$ and $-1.6 \times 10^{-11} \text{ eV m} \leq \beta \leq -4.7 \times 10^{-12} \text{ eV m}$, where e is the unit charge.

superconductivity.^[1,2] The increase of interest in topologically protected qubits has deemed the necessity of investigating novel Si compatible materials supporting topological super-

conductivity. While certain studies have focused on Ge in that context,^[26] the relatively low in-plane g -factor makes it difficult to reach the topological regime. The solution to this problem

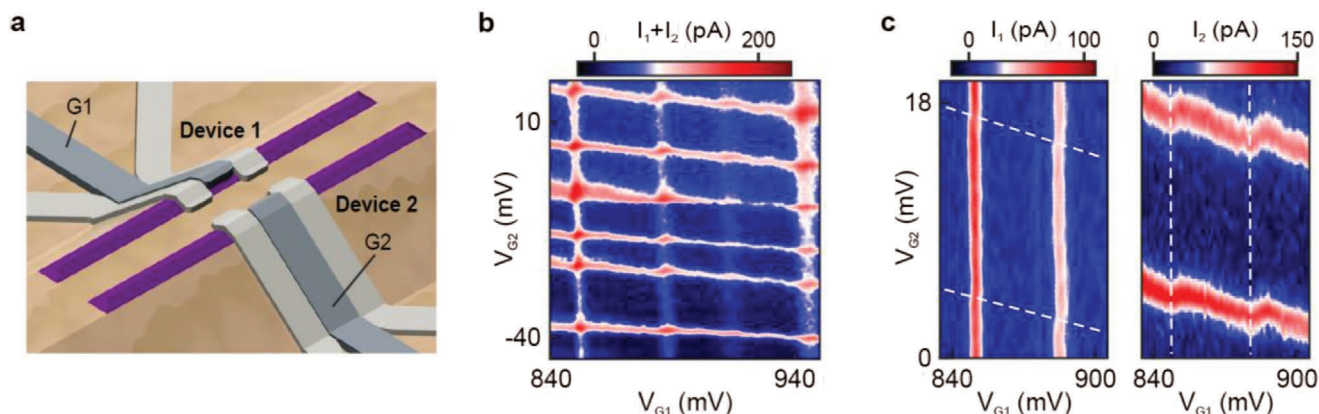


Figure 6. Charge sensing between QDs formed in site-controlled Ge HWs. a) Schematic showing two three-terminal devices (1 and 2) formed from deterministically grown HWs used for investigating the capacitive coupling between them. b) Total current ($I_1 + I_2$) versus V_{G1} and V_{G2} . Whenever a single hole tunneling event takes place in one of the devices, the Coulomb peaks of the other device shift. c) Zoom-in of (b) showing the current through device 1 (left) and device 2 (right). The white dashed lines indicate the positions of the Coulomb peak shifts.

could be to use parallel wires as observed here for which it has been predicted that much smaller, if any, magnetic fields will be needed for reaching the topological regime.^[27] In addition, the Ge wires covered with Si can suppress metallization,^[52] while still allowing proximity induced superconductivity. Finally, the possibility to fabricate wires of arbitrary length, distance, and arrangement is crucial for the realization of a recent proposal for Majorana box qubits,^[53] where braiding of Majorana qubits is not required for universal quantum control. It therefore becomes clear that our site-controlled Ge HWs on Si are systems where aforementioned proposals can be implemented.

Experimental Section

Growth: The trenches were fabricated by electron beam lithography and reactive ion etching on an 8 in. Si (001) wafer. The patterned wafer was cut into $10 \times 10 \text{ mm}^2$ or $16 \times 16 \text{ mm}^2$ small pieces to fit sample adaptors for MBE growth. Before loading into the MBE chamber, the samples were cleaned by the RCA cleaning process and dipped into a 5% hydrogen fluoride (HF) solution for 1 min to remove the oxide layer and form a hydrogen passivated Si surface. The sample dehydrogenation was first performed at 720 °C in the MBE chamber for 10 min. Then, the substrate temperature was ramped down to 450 °C for deposition of a 60 nm Si buffer layer with a growth rate of 1 \AA s^{-1} . The purpose of the homoepitaxial growth of the Si buffer layer was to obtain a high quality surface, which was previously damaged by the top-down fabrication. After the buffer layer, a 3 nm $\text{Si}_{0.75}\text{Ge}_{0.25}$ alloy layer was deposited at 550 °C to form a SiGe mound. The growth rates of Si and Ge were 0.18 and 0.06 \AA s^{-1} , respectively. Keeping the substrate temperature, the Ge growth rate was ramped down to 0.01 \AA s^{-1} within 6 min. Namely, the $\text{Si}_{0.75}\text{Ge}_{0.25}$ alloy layer was annealed for 6 min and this unintentional process ensured a higher quality of the SiGe mound. Next, a 6 Å Ge layer was deposited at 550 °C followed by 1 h in situ annealing. At last, a 3.5 nm Si capping layer was grown at 330 °C with a rate of 1 \AA s^{-1} to protect the Ge HW from oxidation.

Device Fabrication: Three terminal devices were fabricated by means of electron beam lithography, metal, and atomic layer deposition. As source and drain contacts, 25 nm of Pt were evaporated after a HF dip in order to remove the native oxide. For the gate contacts, 3/25 nm of Ti/Pt were deposited on a hafnium oxide layer of 8 nm thickness. In order to demonstrate capacitive coupling of the site-controlled Ge wires, three-terminal devices were fabricated from two parallel grown HWs as illustrated in Figure 6a. Both wires were located at the edges of a plateau and were separated by about 30 nm edge to edge.

All the measurements were done with low-noise electronics and in a He-3/He-4 dilution refrigerator with effective temperature of $\approx 100 \text{ mK}$. All lines were filtered at three stages. Pi filters were used at room temperature, LC filters at the mixing chamber stage, and single stage RC filters on the printed circuit board on which the sample was mounted.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

F.G., J.-H.W., J.-Y.Z., T.W., Y.Y., G.-L.W., and J.-J.Z. performed the substrate patterning, material growth, and characterization experiments. H.W., J.K., L.V., and G.K. fabricated the devices and performed the low temperature transport measurements. H.H. and F.L. developed the growth theory. M.J.R., C.K., and D.L. performed the transport calculations. J.-J.Z. and G.K. planned and designed the experiments.

Keywords

controllable growth, germanium, nanowires, qubits, scalability

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