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2D Materials

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Scratching lithography for wafer-scale MoS₂ monolayers

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Abstract

Monolayer MoS₂ is an emerging two-dimensional (2D) semiconductor with promise on novel electronics and optoelectronics. Standard micro-fabrication techniques such as lithography and etching are usually involved to pattern such materials for devices but usually face great challenges on yielding clean structures without edge, surface and interface contaminations induced during the fabrication process. Here a direct writing patterning approach for wafer-scale MoS₂ monolayers is reported. By controllable scratching by a tip, wafer-scale monolayer MoS₂ films on various substrates are patterned in an ultra-clean manner. MoS₂ field effect transistors fabricated from this scratching lithography show excellent performances, evidenced from a room-temperature on–off ratio exceeding 10^{10} and a high field-effect mobility of 50.7 cm² V⁻¹ s⁻¹, due to the cleanness of as-fabricated devices. Such scratching approach can be also applied to other 2D materials, thus providing an alternate patterning strategy to 2D-materials based devices.

1. Introduction

Monolayer 2H-phase MoS₂, a representative in the two-dimensional (2D) transition metal dichalcogenides (TMDs) family, has recently attracted extensive attentions due to its outstanding physical and chemical properties [1–6]. Such a 2D semiconductor could offer opportunities in many application fields including electronics, optics, optoelectronics and catalysis [7–16]. Usually in MoS₂-based devices processing, standard micro-fabrications, including lithography and reactive ion etching (RIE), are involved. In these fabrication processes, photoresists or electron beam lithography (EBL) resists on the surfaces of these 2D materials are very hard to be removed and harsh reactive ion etching could also cause edge passivations [17, 18]. It is well known that 2D materials are very surface- and interface-sensitive, thus such resists residues or passivations are the main source of quality degradation, acting as additional scattering centers for charge transport [19]. Therefore, a clean micro-fabrication process is needed in order to explore the

intrinsic properties of such monolayers and improve their device performance in many application environments.

Beyond standard micro-fabrications mentioned above, some alternate fabrication approaches, such as the oxidation nanolithography [20–22], peeling-off patterning by gold films [23], laser or argon plasma thinning and patterning [24–26], and micro-molding in capillaries [27], etc, have also been developed for MoS₂. However, due to the chemical reaction process or direct contact of other materials to MoS₂ inevitably involved in these fabrication processes, achieving clean MoS₂ patterns remains a great challenge. Direct nanolithography of 2D materials by atomic force microcopy (AFM) tips or nanoprobes have also been reported previously [28–33], however, the methods are not suitable for wafer-scale patterning.

Aiming to a simple, clean and scalable patterning of MoS₂ monolayers on certain substrates, we here developed a direct writing approach named scratching lithography (SL). In this approach, a metal tip is used to engrave patterns directly by

scratching MoS_2 off within the designed path while keeping the other regions intact. By controlling the tip-scanning path, we are able to achieve various MoS_2 patterns with micro-scale precision. We also show that improved electrical performance can be achieved for SL-patterned MoS_2 field effect transistors (FETs), benefiting from the clean and high-quality as-produced structures.

2. Results and discussions

In this work, wafer-scale highly-oriented monolayer MoS_2 films epitaxially grown on sapphire were used as raw materials for direct patterning [34]. Please see Methods section for detailed materials growth and also figure S1 (available online at https://stacks.iop.org/2DM/7/045028/mmedia) for a typical sample. Figure 1(a) shows our experimental setup installed inside a glovebox. Note that bended tips instead of straight ones were used in order to achieve larger and smoother contact between tip and sample for better reliability and less damages to the underneath substrates. Samples were mounted on a motorized positioning stage, while a metal (tungsten at the present case) tip was mounted on another motorized positioning stage and away from the sample surface. Different from the silicon tips for AFM, tungsten has high hardness, so the tips show a remarkable endurance without crack or deformation. Controlled by stepping motors, both stages can move along *X*-, *Y*- and *Z*- direction with 1 μm precision and 50 mm s^{-1} maximal speed. Sample stages can also rotate and tilt freely with 0.01° precision. In addition, the experimental setup is simple, cost-effective and is suitable to pattern air-degradation sensitive 2D materials such as black phosphorus, magnetic materials and superconducting thin films.

The schematic process of SL is shown in figure 1(b). First, we adjust the stage levelling then slowly lowered the tip until it approaches the sample surface for a direct contact. Before scratching, we tune the tip-to-sample force by the engage distance and the force is estimated to be at the range of 5–10 mN normally. Then, we move either the tip or the sample to start scratching along any predesigned paths. Because of the weak binding force between MoS_2 and substrates, it is easy to fully tear and scratch MoS_2 off within the scanning paths. It is worth noting that the stability and levelness of positioning stages are two major factors for clean, straight and sharp scratched patterns; while the tip's moving speed has no obvious influence on it. The minimum line width of the scratched ribbons or grooves depends on both the precision of stepping motors and the tip-to-sample contact area (about 10 μm^2 at the present case). After scratching, various patterns of monolayer MoS_2 at a wafer-scale can be achieved. Please also see the supplementary video 1 & 2 for a better illustration.

Figure 1(c) shows a 2 inch MoS_2/sapphire sample after series of line scratching. After scratching, most of the MoS_2 residues accumulated at the end of paths on the samples (refer to upper image of figure 1(d)), while the residues were hardly observed on the tip. Therefore it is no need to clean the tip during the scratching process unless a block of residues stick on it by accident. After every runs of experiments, we sonicated the tip in alcohol for cleaning. These residues on the samples can be completely removed by post gentle sonication in alcohol (refer to lower image of figure 1(d)), as confirmed from the barely unchanged Raman and photoluminescence (PL) spectra on the MoS_2 sample areas and no signals on the scratched areas (figures 1(e) & (f)). Moreover, the sonication makes no obvious difference on the quality of monolayer MoS_2. Please see figure S2 for more detailed information. Combining the scratching and sonication process, we thus are able to obtain various clean MoS_2 patterns, such as ribbons, squares, chessboards and numbers as shown in figure 1(g). Note that monolayer MoS_2 has strong fluorescence intensity due to its direct bandgap [3]. The high-contrast fluorescence microscopy image shown in figure 1(h) confirms again the cleanness and preserved optical quality of as-fabricated structures. The scratched patterns possess clean surfaces and sharp edges as shown in AFM image (figure 1(i)). A minimum line width of 1 micron, which is comparable to the accuracy of a standard ultraviolet (UV)-lithography, can be achieved reliably (refer to figure S3 for more details). Figure 1(j) shows the distribution of channel width for SL patterned 1 μm ribbons and over 35% ribbons are measured with the width between 0.95 μm and 1.05 μm. Actually, the precision could be much higher if improving the precision of stepping motors or including a feedback for tip-engaging to reduce the contact area between the tip and sample.

Based on these scratched monolayer MoS_2 microstructures, we thus fabricated field effect transistors to demonstrate the potential of such clean structures. In order to avoid a secondary contamination, we developed a lithography-free device fabrication process as shown in figure 2(a). In this process, monolayer MoS_2 films were firstly transferred from sapphire substrates onto SiO_2/Si substrates via a water-assisted transfer method [34]. SL was then followed to separate and define the MoS_2 channels. Gold electrodes with a thickness of 40 nm were pre-deposited on poly propylene carbonate (PPC) by an electron beam evaporation system with the aid of a shadow mask. Finally, the electrodes were aligned and dry-transferred from PPC to the MoS_2 channels on SiO_2/Si substrates. Please see more detailed description of fabrication process in supporting information (figures S4-S6). Note that the whole process is lithography-free without any photoresist. Here we choose the transferred electrodes, because direct evaporation of metal films on
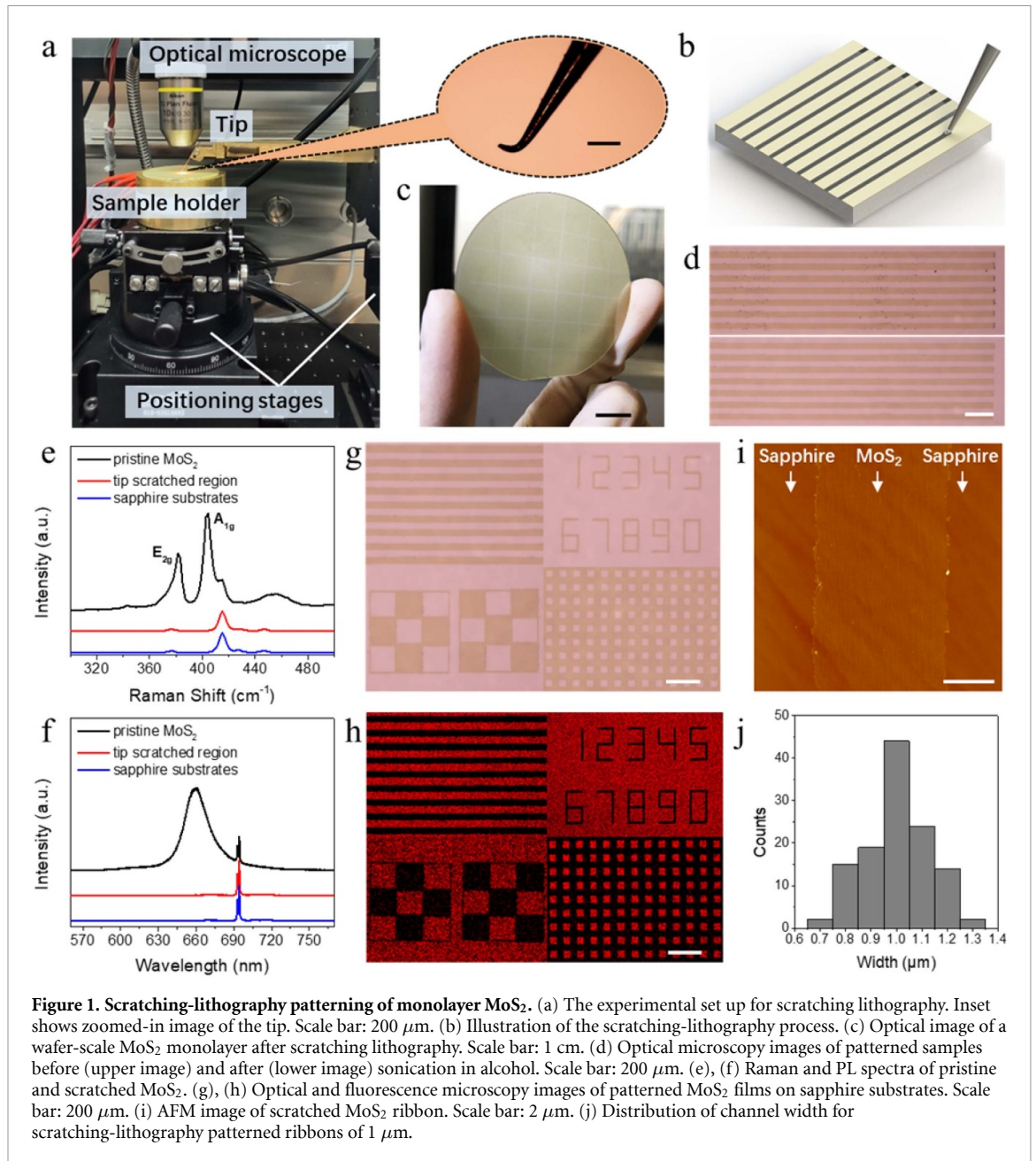
Figure 1. Scratching-lithography patterning of monolayer MoS₂. (a) The experimental set up for scratching lithography. Inset shows zoomed-in image of the tip. Scale bar: 200 μm. (b) Illustration of the scratching-lithography process. (c) Optical image of a wafer-scale MoS₂ monolayer after scratching lithography. Scale bar: 1 cm. (d) Optical microscopy images of patterned samples before (upper image) and after (lower image) sonication in alcohol. Scale bar: 200 μm. (e), (f) Raman and PL spectra of pristine and scratched MoS₂. (g), (h) Optical and fluorescence microscopy images of patterned MoS₂ films on sapphire substrates. Scale bar: 200 μm. (i) AFM image of scratched MoS₂ ribbon. Scale bar: 2 μm. (j) Distribution of channel width for scratching-lithography patterned ribbons of 1 μm.
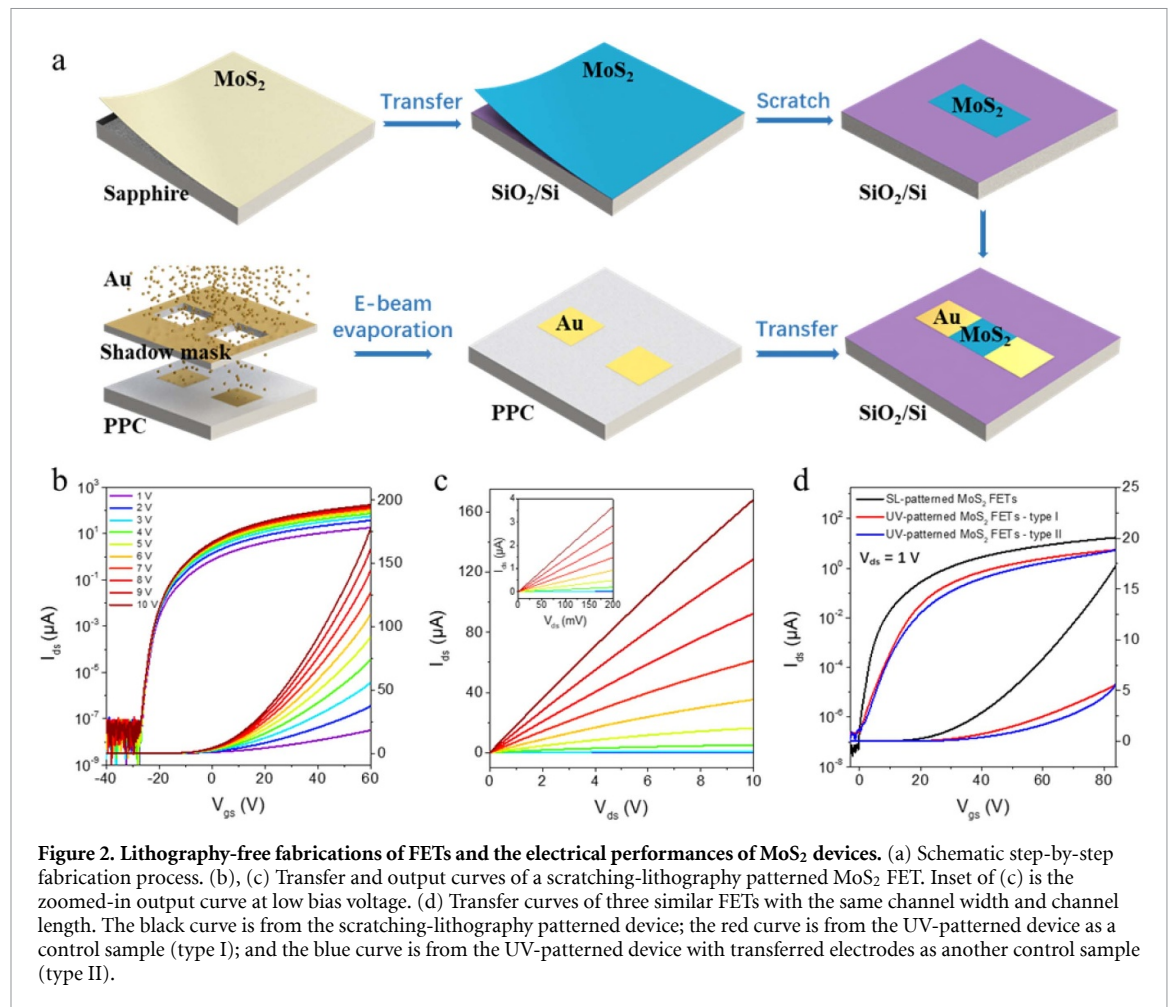
MoS₂ could cause structure damages, due to the bombardment from high energy metal atoms and clusters, thus degrade the contact quality [35]. This lithography-free device fabrication process might be also applicable to other fragile and contamination-sensitive materials like biologic or organic materials.

Next, we measured the electrical performance of these as-fabricated devices in a high vacuum four-probe station system. Figures 2(b)–(c) show the transfer and output characteristics of a typical FET with both the channel length L and width W of 27 μm. From the output characteristics, it shows that the source-drain current I_{ds} changes linearly with the bias voltage V_{ds} when varying the gate voltage V_{gs} from $-$ 30 V to 60 V, suggesting nearly ohmic contacts. In the transfer characteristics of the same transistor, a typical n-type behavior and high on-off ratio

exceeding 10^{10} can be clearly seen. According to the equation $\mu = \left[dI_{ds}/dV_{gs}\right] \times \left[L/(WC_iV_{ds})\right]$, where μ is the field-effect mobility and C_i is the capacitance of the dielectric layer per unit area [8], we obtained $\mu = 50.7$ cm^2 V^{-1} s^{-1} at the room temperature. Note that the SL patterned device shows excellent electrical performances, for example higher current on-off ratio and field-effect mobility than previous works [9, 34, 36].

We also fabricated two types of control samples for a better comparison. In type-I devices, monolayer MoS₂ was patterned by UV-lithography and RIE; in the following, electrodes were deposited by electron beam evaporation. In type-II devices, monolayer MoS₂ was patterned by UV-lithography and RIE; and electrodes were transferred instead of direct deposition. The transfer and output characteristic curves of
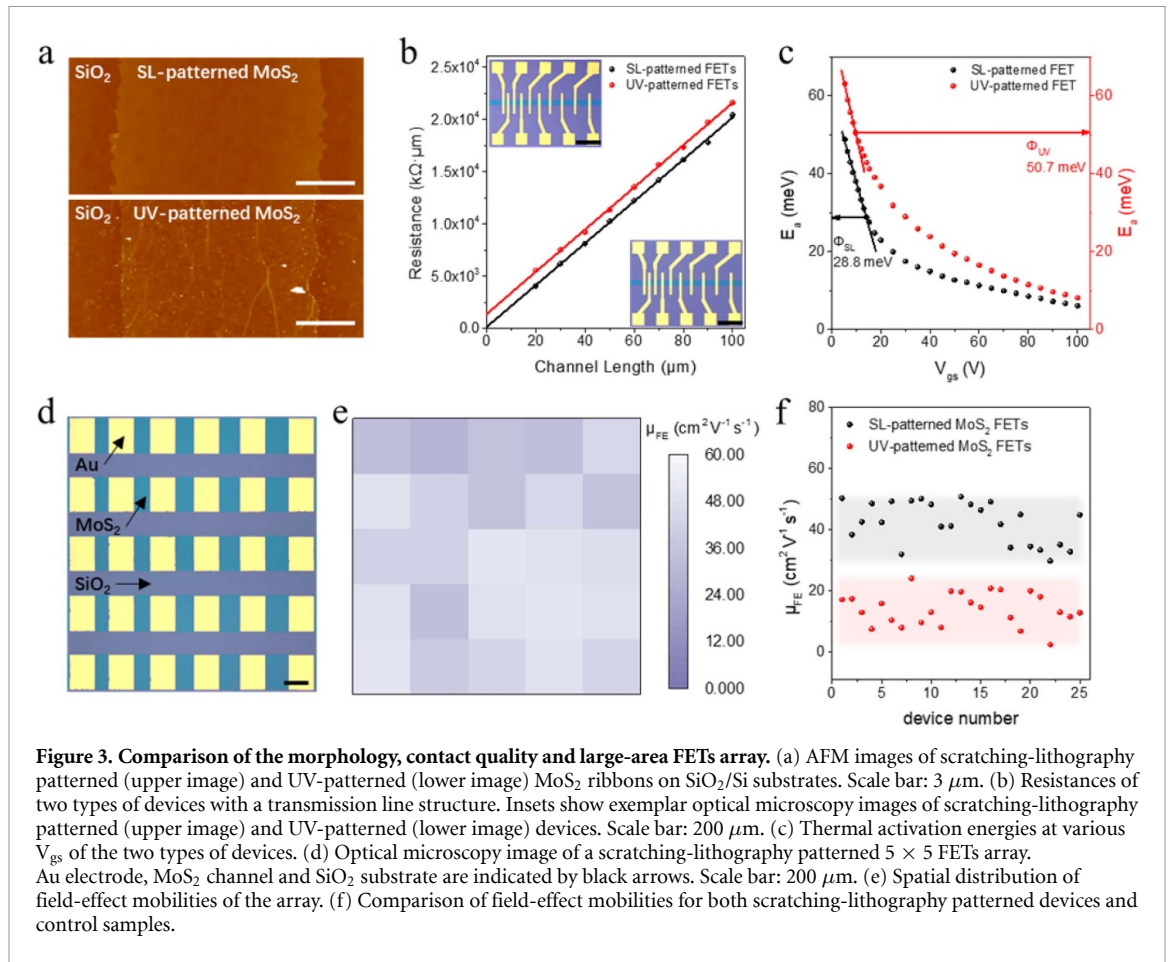
Figure 2. Lithography-free fabrications of FETs and the electrical performances of MoS₂ devices. (a) Schematic step-by-step fabrication process. (b), (c) Transfer and output curves of a scratching-lithography patterned MoS₂ FET. Inset of (c) is the zoomed-in output curve at low bias voltage. (d) Transfer curves of three similar FETs with the same channel width and channel length. The black curve is from the scratching-lithography patterned device; the red curve is from the UV-patterned device as a control sample (type I); and the blue curve is from the UV-patterned device with transferred electrodes as another control sample (type II).

the two types of control transistors with L = 30 μm and W = 30 μm are shown in figure S7(a)–S7(d), respectively. The output curves of control samples show ohmic contacts but lower source-drain current compared with the SL-patterned transistor. Lower on–off ratios of ~10^7 (at a bias of 1 V) can be seen for both control devices. Figure 2(d) shows transfer characteristic curves at V_{ds} = 1 V of three different types of devices with same L and W. Note that we shifted the threshold voltage of all curves to 0 V for better comparisons. We can see clearly that the SL-patterned transistor shows higher on-state current and lower off-state current, leading to a higher on-off ratio and field-effect mobility. The two types of control samples show similar electrical properties and the field-effect mobility of them are much lower, i.e. 13.05 cm^2 V^{-1} s^{-1} and 17.40 cm^2 V^{-1} s^{-1} for type I and type II, respectively. Larger hysteresis can also be seen in figure S8 in control devices, due to the presence of surface or edge contaminations, which act as charge-trapping centers [37].

We attribute the excellent electrical performance of SL-patterned FETs to the clean surfaces and interfaces of our devices. To verify this point of view, we characterized SL- and UV-patterned MoS₂ strips by AFM. From the AFM images shown in figure 3(a), we can see that the SL-patterned samples

are much cleaner at surfaces; while a plenty of residues/contaminations and structure deformations can be seen in the UV-patterned samples, even after a long period of thermal annealing or rinsing in acetone. In spite of the channel, the excellent electrical performance of SL-patterned FETs may also be benefited from the ultra-clean contact region and transferred electrodes. Contact resistance (R_c) and Schottky barrier height (SBH) were measured on many devices. In R_c measurements, we fabricated MoS₂ FETs with transmission line structure (inset of figure 3(b)) and estimated R_c according to the transfer length method (TLM) [38]. Figure 3(b) gives the comparison of R_c between the SL-patterned and UV-patterned FETs (type I), and the resulted R_c is 63.2 k$\Omega \cdot \mu$m and 688.8 k$\Omega \cdot \mu$m, respectively. SBH of these two contacts were extracted from the Arrhenius plots show in figure S9 [39, 40]. Figure 3(c) shows the resulted SBH = 28.8/50.7 meV for the SL-/UV- patterned MoS₂ FETs. Near one order of magnitude lowered R_c and almost halved Schottky barrier height in such clean devices contribute to their high performances compared with those of the traditional UV-patterned devices in no doubt.

Figure 3(d) shows a 5 × 5 array of SL-patterned FETs. Corresponding spatial distribution of field-effect mobility of this array is shown in figure 3(e),

Figure 3. Comparison of the morphology, contact quality and large-area FETs array. (a) AFM images of scratching-lithography patterned (upper image) and UV-patterned (lower image) MoS$_2$ ribbons on SiO$_2$/Si substrates. Scale bar: 3 μm. (b) Resistances of two types of devices with a transmission line structure. Insets show exemplar optical microscopy images of scratching-lithography patterned (upper image) and UV-patterned (lower image) devices. Scale bar: 200 μm. (c) Thermal activation energies at various V$_{gs}$ of the two types of devices. (d) Optical microscopy image of a scratching-lithography patterned 5 × 5 FETs array. Au electrode, MoS$_2$ channel and SiO$_2$ substrate are indicated by black arrows. Scale bar: 200 μm. (e) Spatial distribution of field-effect mobilities of the array. (f) Comparison of field-effect mobilities for both scratching-lithography patterned devices and control samples.

indicating a high uniformity in device performances. The optical microscopy image of another 5 × 5 array of the UV-lithography patterned FETs (control samples) and the corresponding spatial distribution of mobility are shown in figure S10(a)–(b), respectively. Comparison of field-effect mobility between 25 SL-patterned FETs and 25 UV-patterned FETs are shown in figure 3(f). Mobilities of the UV-patterned FETs vary from 2.46 cm^2 V^{-1} s^{-1} to 24.09 cm^2 V^{-1} s^{-1} and average at 14.09 cm^2 V^{-1} s^{-1}; while mobilities of the SL-patterned FETs vary from 29.85 cm^2 V^{-1} s^{-1} to 50.85 cm^2 V^{-1} s^{-1} and average at 42.43 cm^2 V^{-1} s^{-1}. Obviously, the SL-fabricated devices have improved electronic qualities. These results reveal the importance of the structural cleanness on the device performance.

SL is also applicable to other 2D materials or even thick films. Figures 4(a)–(j) show optical microscopy images of various SL-patterned films on different substrates. The films include monolayer and bilayer MoS$_2$, 3 nm gold, 3 nm nano-graphene, 30 nm Al$_2$O$_3$, polymethyl methacrylate (PMMA), 5 nm Sn, and exfoliated graphene, few-layer BN and few-layer MoS$_2$. The substrates used are SiO$_2$/Si, Si and sapphire. Note that SL approach shows applicability in the fabrication of ultra-clean homostructures and heterostructures as well. Figures 4(k)–(m) show

optical microscopy images of MoS$_2$ homostructures and MoS$_2$/graphene heterostructures which are prepared by stacking pre-scratched strips layer-by-layer. Similarly, SL shows promise in the fabrication of 2D material based p-n junctions or superlattices. In figure S11, we also tested MoS$_2$ or nano-graphene films on SiO$_2$/Si, sapphire and flexible polyethylene terephthalate (PET) substrates. All fabricated structures are of preserved quality with ultra-clean surfaces and sharp edges, suggesting the versatility of this approach.

3. Conclusion

In this work, we developed a simple, clean and scalable approach to pattern monolayer MoS$_2$. This SL approach offers a minimum line width of $\sim$1 μm. Clean MoS$_2$ FETs were fabricated by this approach and show improved electrical properties than those of lithography and etching defined devices, revealing the advances of this new approach. This approach is also applicable to other 2D materials on various substrates, thus paving a way towards facile fabrication of large-scale high-performance 2D-materials based electronic or optoelectronic devices.
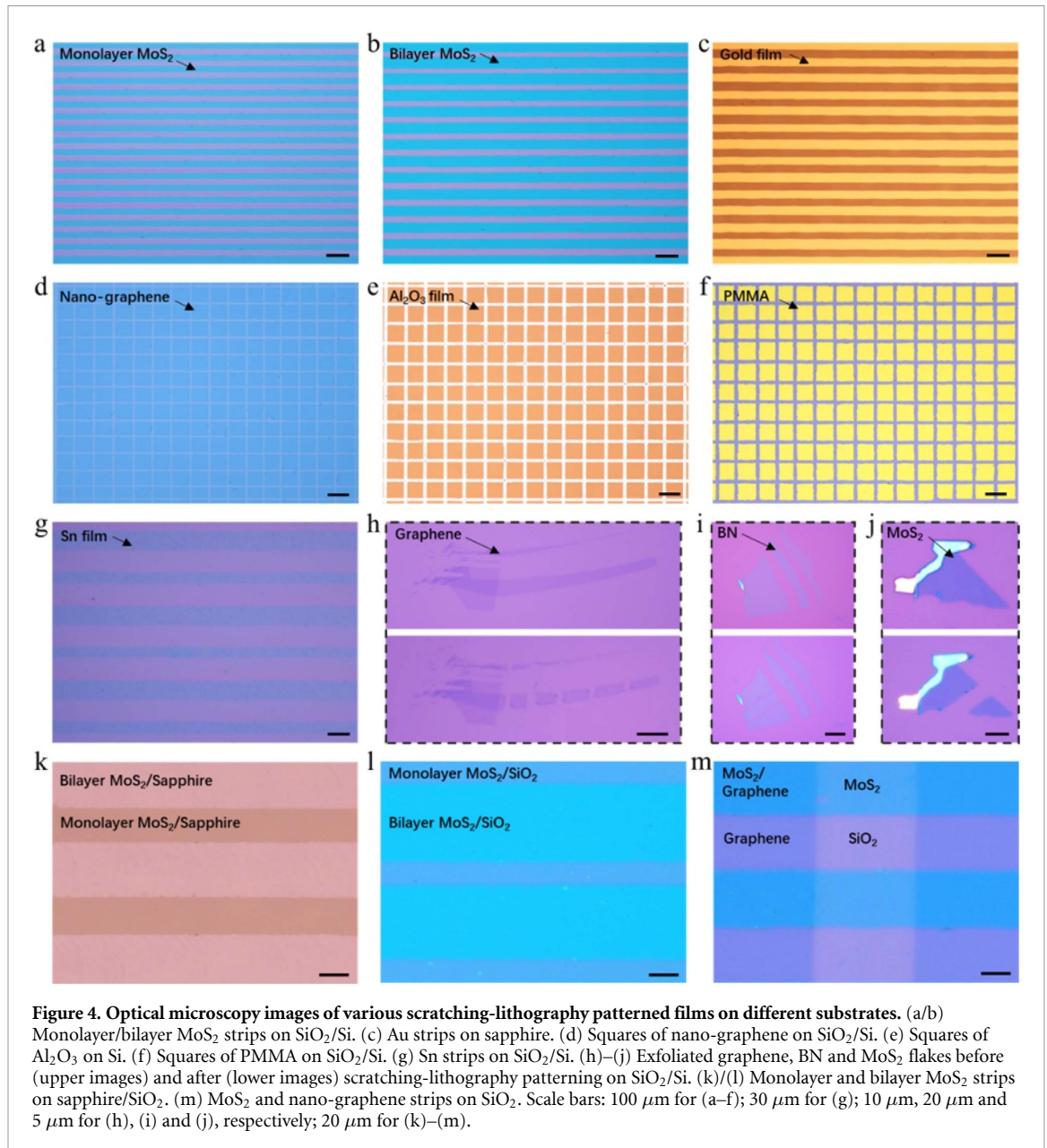
Figure 4. Optical microscopy images of various scratching-lithography patterned films on different substrates. (a/b) Monolayer/bilayer MoS_2 strips on SiO_2/Si. (c) Au strips on sapphire. (d) Squares of nano-graphene on SiO_2/Si. (e) Squares of Al_2O_3 on Si. (f) Squares of PMMA on SiO_2/Si. (g) Sn strips on SiO_2/Si. (h)–(j) Exfoliated graphene, BN and MoS_2 flakes before (upper images) and after (lower images) scratching-lithography patterning on SiO_2/Si. (k)/(l) Monolayer and bilayer MoS_2 strips on sapphire/SiO_2. (m) MoS_2 and nano-graphene strips on SiO_2. Scale bars: 100 μm for (a–f); 30 μm for (g); 10 μm, 20 μm and 5 μm for (h), (i) and (j), respectively; 20 μm for (k)–(m).

4. Methods

4.1 Wafer-scale MoS_2 growth

The growth was carried out in a three-temperature-zone chemical vapor deposition (CVD) system with the schematic shown in figure S1(a). S (Alfa Aesar, 99.5%, 5 g) and MoO_3 (Alfa Aesar, 99.999%, 10 mg) powders were loaded in two inner quartz tubes at zone I and zone II, respectively, as reaction sources. Pre-annealed 2 inch sapphire wafers (C-plane off M-axis, thickness: 430 μm) were used as substrates and placed at high-temperature zone III. During the growth process, temperatures at zone-I, zone-II and zone-II were 130 °C, 530 °C and 900 °C, respectively; and Ar (200 sccm) and Ar/O_2 (75 sccm/3.5 sccm) were flowed through the inner tubes for the S-source and MoO_3-source, respectively, as carrying gases. Here, O_2 can prevent the sulfurization of MoO_3 thus guarantee a continuous evaporation and reduce the nucleation density as well. The pressure of the growth chamber was kept at $\sim$ 1 Torr, and the whole growth process lasted for 45 min.

4.2 Characterizations of samples

AFM imaging of SL-patterned samples and UV-patterned samples were performed by Veeco Multimode III system under the tapping mode. Raman and PL spectra were performed by Horiba Jobin Yvon LabRAM HR-Evolution Raman system with a 532 nm laser excitation under a power of 500 μW and the integral time were 5 s and 10 s, respectively. Fluorescence microscopy images were collected by Olympus confocal fv3000 microscope with an exposure time of 100 ms.

4.3 Device fabrications and measurements

Control samples were fabricated by the standard micro-fabrication process. The transferred monolayer MoS_2 samples were first patterned into ribbons by UV lithography (Suss MicroTec Gmbh MA6) and RIE (Oxford Instruments Plasma 80 plus). Gold electrodes were patterned by a second UV lithography process and deposited by electron beam evaporation with thickness of 40 nm. Electrical measurements on all the devices were carried out in a high-vacuum $(1 \times 10^{-6}$ mbar) four-probe-station system by an Agilent 4156 C semiconductor parameter analyzer.

4.4 Preparation of other film materials

Monolayer MoS_2 films on SiO_2/Si substrates were grown by CVD with a deposition temperature of 750 °C. Bilayer MoS_2 films SiO_2/Si were transferred layer-by-layer from sapphire substrates. Au films on sapphire were deposited by electron beam evaporation. Nano-graphene on SiO_2/Si was grown by plasma-enhanced CVD (CH_4 as source) with a deposition temperature of 560 °C. Al_2O_3 films on Si substrates were fabricated by standard atomic layer deposition. PMMA films on SiO_2/Si were fabricated by spin-coating with a rotate speed of 4000 r min^{-1} and followed by a heating process at 180 °C. Sn films on SiO_2/Si were prepared by squeegee method at 260 °C. Exfoliated graphene, BN and MoS_2 films were cleaved from bulk materials by Scotch tape and transferred onto SiO_2/Si substrates.

Author contributions

G Z supervised the project. Z W and Q W prepared the MoS_2 samples and J T prepared the nano-graphene samples. Y Z and Y C prepared the exfoliated graphene, BN and MoS_2 samples and J L prepared the Sn samples. M L set up the positioning system. Y G fabricated the shadow masks. Y C wrote the programme for automatic stage control. H C draw the schematic illustration of the device nobreakfabrication process. Q J and Y L performed the fluorescence mapping. Z W carried out patterning of the films, fabrication of the devices and spectroscopic and electrical measurements. G Z and Z W analysed the results and wrote the manuscript. All authors commented on this paper.

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References

[1] Mak K F, Lee C, Hone J, Shan J and Heinz T F 2010 *Phys. Rev. Lett.* **105** 136805
[2] Lee C, Yan H, Brus L E, Heinz T F, Hone J and Ryu S 2010 *ACS Nano* **4** 2695–700
[3] Splendiani A, Sun L, Zhang Y, Li T, Kim J, Chim C Y, Galli G and Wang F 2010 *Nano Lett.* **10** 1271–5
[4] Chhowalla M, Shin H S, Eda G, Li L J, Loh K P and Zhang H 2013 *Nat. Chem.* **5** 263–75
[5] Xu M, Liang T, Shi M and Chen H 2013 *Chem. Rev.* **113** 3766–98
[6] Lee J, Wang Z, Xie H, Mak K F and Shan J 2017 *Nat. Mater.* **16** 887–91
[7] Wang Q H, Kalantar-Zadeh K, Kis A, Coleman J N and Strano M S 2012 *Nat. Nanotechnol.* **7** 699–712
[8] Radisavljevic B, Radenovic A, Brivio J, Giacometti V and Kis A 2011 *Nat. Nanotechnol.* **6** 147–50
[9] Lin Z *et al* 2018 *Nature* **562** 254–8
[10] Shinde S M, Das T, Hoang A T, Sharma B K, Chen X and Ahn J-H 2018 *Adv. Funct. Mater.* **28** 1706231
[11] Voiry D *et al* 2016 *Nat. Mater.* **15** 1003–9
[12] Lopez-Sanchez O, Lembke D, Kayci M, Radenovic A and Kis A 2013 *Nat. Nanotechnol.* **8** 497–501
[13] Wu W *et al* 2014 *Nature* **514** 470–4
[14] Feng J, Graf M, Liu K, Ovchinnikov D, Dumcenco D, Heiranian M, Nandigana V, Aluru N R, Kis A and Radenovic A 2016 *Nature* **536** 197–200
[15] Xie L *et al* 2017 *Adv. Mater.* **29** 1702522
[16] Zhao J *et al* 2017 *Adv. Mater.* **29** 1702076
[17] Liang J, Xu K, Toncini B, Bersch B, Jariwala B, Lin Y-C, Robinson J and Fullerton-Shirey S K 2019 *Adv. Mater. Interfaces* **6** 1801321
[18] Freedy K M, Sales M G, Litwin P M, Krylyuk S, Mohapatra P, Ismach A, Davydov A V and McDonnell S J 2019 *Appl. Surf. Sci.* **478** 183–8
[19] Li S L, Tsukagoshi K, Orgiu E and Samori P 2016 *Chem. Soc. Rev.* **45** 118–51
[20] Li H, Ying Z, Lyu B, Deng A, Wang L, Taniguchi T, Watanabe K and Shi Z 2018 *Nano Lett.* **18** 8011–5
[21] Espinosa F M, Ryu Y K, Marinov K, Dumcenco D, Kis A and Garcia R 2015 *Appl. Phys. Lett.* **106** 103503
[22] Donarelli M, Perrozzi F, Bisti F, Paparella F, Feyer V, Ponzoni A, Gonchigsuren M and Ottaviano L 2015 *Nanoscale* **7** 11453–9
[23] Zhao J, Yu H, Chen W, Yang R, Zhu J, Liao M, Shi D and Zhang G 2016 *ACS Appl. Mater. Interfaces* **8** 16546–50
[24] Hu L, Shan X, Wu Y, Zhao J and Lu X 2017 *Sci. Rep.* **7** 15538
[25] Liu Y, Nan H, Wu X, Pan W, Wang W, Bai J, Zhao W, Sun L, Wang X and Ni Z 2013 *ACS Nano* **7** 4202–9
[26] Castellanos-Gomez A, Barkelid M, Goossens A M, Calado V E, van der Zant H S and Steele G A 2012 *Nano Lett.* **12** 3187–92

[27] Hung Y H, Lu A Y, Chang Y H, Huang J K, Chang J K, Li L J and Su C Y 2016 *ACS Appl. Mater. Interfaces* **8** 20993–1001

[28] Ye S *et al* 2018 *Mater. Res. Express* **6** 025048

[29] Li B *et al* 2010 *Adv. Mater.* **22** 3058–61

[30] Tran Khac B C, DelRio F W and Chung K H 2018 *ACS Appl. Mater. Interfaces* **10** 9164–77

[31] Kumar V, Mehdizadeh E and Pourkamali S 2016 *IEEE Trans. Nanotechnol.* **15** 457–64

[32] Dago A I, Ryu Y K, Palomares F J and Garcia R 2018 *ACS Appl. Mater. Interfaces* **10** 40054–61

[33] Rani E and Wong L S 2019 *Adv. Mater. Technol.* **4** 1900181

[34] Yu H *et al* 2017 *ACS Nano* **11** 12001–7

[35] Liu Y, Guo J, Zhu E, Liao L, Lee S-J, Ding M, Shakir I, Gambin V, Huang Y and Duan X 2018 *Nature* **557** 696–700

[36] Li Y, Ye F, Xu J, Zhang W, Feng P X L and Zhang X 2018 *IEEE Trans. Electron Devices* **65** 4068–72

[37] Choi M S, Lee G H, Yu Y J, Lee D Y, Lee S H, Kim P, Hone J and Yoo W J 2013 *Nat. Commun.* **4** 1624

[38] Kappera R, Voiry D, Yalcin S E, Branch B, Gupta G, Mohite A D and Chhowalla M 2014 *Nat. Mater.* **13** 1128–34

[39] Radisavljevic B and Kis A 2013 *Nat. Mater.* **12** 815–20

[40] Das S, Chen H Y, Penumatcha A V and Appenzeller J 2013 *Nano Lett.* **13** 100–5