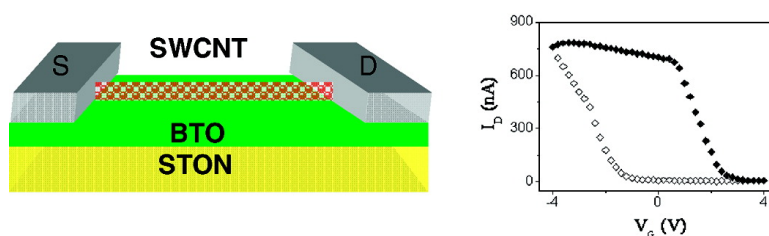


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# Intrinsic Memory Function of Carbon Nanotube-based Ferroelectric Field-Effect Transistor

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## ABSTRACT

We demonstrate the intrinsic memory function of ferroelectric field-effect transistors (FeFETs) based on an integration of individual single-walled carbon nanotubes (SWCNTs) and epitaxial ferroelectric films. In contrast to the previously reported “charge-storage” CNT-FET memories, whose operations are haunted by a lack of control over the “charge traps”, the present CNT-FeFETs exhibit a well-defined memory hysteresis loop induced by the reversible remnant polarization of the ferroelectric films. Large memory windows  $\sim 4$  V, data retention time up to 1 week, and ultralow power consumption (energy per bit) of  $\sim$  femto-joule, are highlighted in this report. Further simulations and experimental results show that the memory device is valid under operation voltage less than 1 V due to an electric-field enhancement effect induced by the ultrathin SWCNTs.

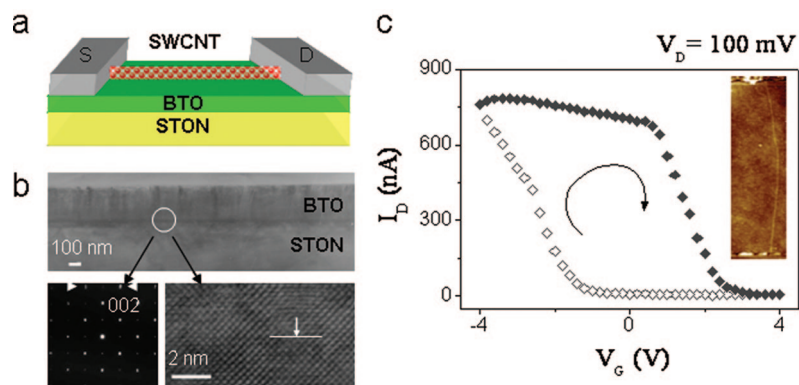
Single-walled carbon nanotubes (SWCNTs)<sup>1–6</sup> are perfect one-dimensional (1D) nanostructures that exhibit unique physical and chemical properties, such as extremely high chemical stability (no dangling bonds), mechanical robustness, and room-temperature ballistic transport. In the past decade, CNTs have been actively integrated as key component of the ubiquitous field-effect transistors (FETs) that witnessed tremendous advancement in both device fabrication and characteristics. CNT-FETs also demonstrated potentials for room temperature single- or few-electron “charge-storage” memories in 2002.<sup>7,8</sup> Afterward, researches on improvement of the charge storage stability (up to 12 days) and adoption of charge traps such as floating metal nanocrystal gate or SiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub>/SiO<sub>2</sub> trilayer<sup>9–11</sup> were reported. Optoelectronic<sup>12</sup> and multibit<sup>13</sup> CNT memory devices, based on the hysteresis effect, have also been demonstrated recently. These achievements have significantly extended the applications of CNTs used for memories. However, efforts to date have mainly been focused on the so-called “charge-storage” effect, in which an electron percolation path in the nanotube forms the channel, and the charge traps (such as interface water molecules,<sup>14</sup> metal nanocrystals, and defects) near the conduction path act as the floating gate. Such structures intrinsically prevent precise control of the placement and dimension for charge traps and tunnel barrier. The resulting lack of control over the threshold voltage shift

(memory window) thus the memory switch makes it undesirable for any practical applications.

One solution is to replace the uncontrollable charge traps with ferroelectrics that exhibit a well-defined reversible spontaneous polarization, thus to develop a FeFET memory.<sup>15–23</sup> It remains a challenge to demonstrate the intrinsic function and the most attractive performance of such a CNT-FeFET memory unit, which are represented by controllable switching, nondestructively read-out (NDRO) operation, long data retention time, low electric power consumption, high carrier mobility, and so forth. Sakurai et al. reported the CNT-FETs<sup>24</sup> with a nonvolatile memory function using ferroelectric dielectrics. However, the inferior FET characteristics make it difficult to determine the memory performance of the devices. Ferroelectric materials have also been used as high- $\kappa$  insulators for CNT-FETs that showed improved electrical characteristics,<sup>25</sup> but no ferroelectric memory effect was reported.

Here, we present the CNT-FeFET memory based on an integration of individual SWCNTs and high-quality epitaxial ferroelectric films. The prototype device exhibits a controllable memory switch behavior induced by the reversible remnant polarization of the ferroelectric films and also a NDRO operation. Data retention as long as 1 week, large memory windows  $\sim 4$  V, and ultralow power consumption (energy per bit) of  $\sim$  femto-joule are demonstrated. Further results show that the memory device is valid under operation voltage less than 1 V due to an electric-field enhancement effect induced by the nanometer-diameter SWCNTs.

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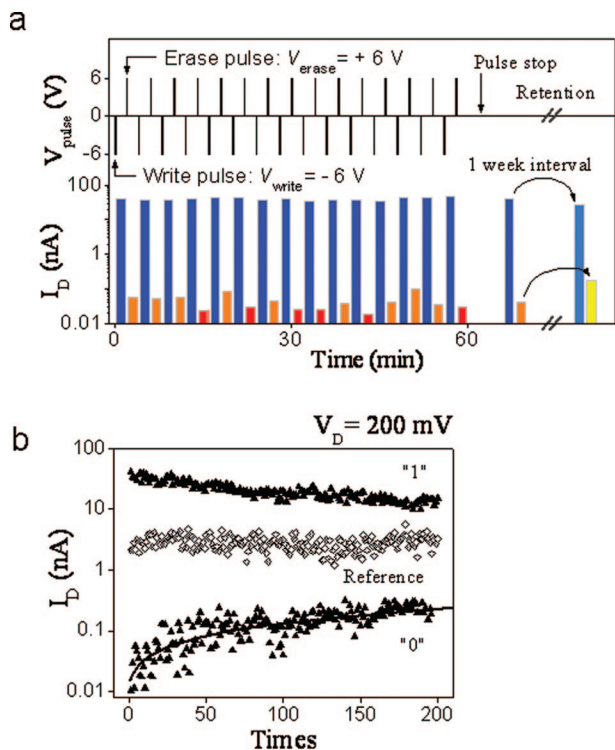


**Figure 1.** (a) Schematic sketch of the fabricated CNT-FeFET. (b) Structural characterization of BaTiO<sub>3</sub> thin films deposited on STON substrates by TEM, indicating the coherent epitaxial growth of BaTiO<sub>3</sub> thin film with respect to STON substrate. (c) Typical  $I_D$ – $V_G$  transfer characteristics of the CNT-FeFET made of SWCNT with 600 nm in length. The arrows indicate a clockwise hysteresis loop.

A number of challenges are included in achieving a CNT-FeFET. First, any trapped charges near the CNT channel could lead to local charge compensation thus degenerate the effect of polarization. As a result, the intrinsic ferroelectric memory function of CNT-FeFETs can only be achieved with high-quality ferroelectric films that lack defects around the CNT surface and have improved interface between the CNT and ferroelectric film. We prepared a 300 nm thick epitaxial ferroelectric BaTiO<sub>3</sub> film with smooth surface on a single crystal Nb-doped (001) SrTiO<sub>3</sub> (STON) substrate as a gate dielectric (Figure 1a). The deposition was carried out in 10 Pa of O<sub>2</sub> at 750 °C by pulsed laser deposition (PLD). An in situ post annealing was followed at 550 °C in oxygen ambient of 1 bar for 30 min to neutralize the oxygen vacancy and improve the crystallization of the thin film after deposition. The cube-on-cube epitaxy nature and the smooth surface with root-mean-square (rms) roughness of less than 0.4 nm of the as-annealed ferroelectric film was confirmed by the high-resolution transmission electron microscopy (TEM) (Figure 1b) and atomic force microscopy (see Supporting Information, Figure S1). Second, high temperature and oxygen are always included in the deposition process for high-quality ferroelectric films, so it is very difficult to deposit ferroelectric films directly onto CNT surface. We developed an alternative method to solve this problem, that is, to put CNT onto ferroelectric. Thus, for FET device fabrication, the SWCNTs prepared by plasma-enhanced chemical vapor deposition (PECVD)<sup>26</sup> with diameter ~1 nm were sonicated into a suspension in a dimethylformamide solution and then deposited onto the prepared ferroelectric films by a spin-on technique followed by baking at 180 °C for 90 min. Electron beam lithograph (EBL), Pt deposition, and a lift-off technique were used for source and drain electrode formation. Here again, a process of prebaking at 180 °C for 90 min was required before measurements to minimize the potential charge traps (for example, water molecules adsorption) on CNT surfaces. Electrical transport measurements of the CNT-FeFETs are performed by a Keithley 6487/2400 joint setup at room temperature in dry air. The STON substrate is served as back gate (Figure 1a). Dozens of the devices were fabricated and tested.

Figure 1c shows typical  $I_D$ – $V_G$  transfer characteristic, which are stamped by a “clockwise” hysteresis loop when the gate voltage sweeps upward (from negative to positive) and downward continuously. The device acts as a *p*-type Schottky-barrier transistor. The threshold voltage ( $V_{th}$ , defined as the gate voltage at which the SWCNT channel begins to conduct) has changed from ~2.5 to ~–1.5 V as the gate voltage sweeps upward and downward, giving a large memory window  $\Delta V_{th}$  of 4 V with a wide drain current plateau of both on- and off-states. Such clockwise hysteresis loops is in satisfactory agreement with the nonvolatile memory operation induced by the ferroelectric films as expected. The transconductance,  $g_m = I_D/V_G$ , is ~400 nA V<sup>–1</sup>, and the hole carrier mobility of about 260 cm<sup>2</sup> V<sup>–1</sup> s<sup>–1</sup> is of orders of magnitude larger than those of the conventional oxide-semiconductor or organic FeFETs (several cm<sup>2</sup> V<sup>–1</sup> s<sup>–1</sup> or less).<sup>15,19</sup> It is estimated that the energy consumption per bit is on the level of 10<sup>–15</sup> J in the case of a FeFET unit with a 600 nm SWCNT channel, which is significantly lower than that of the latest developed ultralow power phase-change nanowire memory.<sup>27</sup> For the ultimate speed of the devices, the ballistic traversal time and resistance-capacitance time<sup>2</sup> for the 600 nm length tube are both of ~10<sup>–12</sup> s (or 1 THz). Thus the frequency limit is given by the switch time of the ferroelectrics which can be ~10<sup>–10</sup> s (or 10 GHz).

The clockwise hysteresis loop mentioned above can be used for FeFET memory devices, that is, the modulation of the threshold voltages by the stored dipole moments in the ferroelectric film would lead to discriminated drain currents of each logic switch state in a memory. A typical device test is shown in Figure 2a with controllable, nonvolatile memory switching characteristics. During the test, the drain voltage was set as 200 mV, and voltage pulses with 0.1 ms width were applied between the gate and the source to polarize the ferroelectric film underneath the nanotube. An on- and an off-state drain currents of ~40 and ~0.02 nA can be switched with a write and an erase gate voltage pulses of –6 and +6 V ( $V_D$  = 200 mV) in a controllable manner, respectively. When repeating the write/erase operations, the measured on/off ratio were kept on ~10<sup>3</sup> with only a little deviation. Within the period up to one week, we tested the



**Figure 2.** Intrinsic memory function of CNT-FeFETs. (a) Retentive write/erase operation, showing the controllable, nonvolatile memory switching of the CNT-FeFETs. The on- and an off-state drain currents of  $\sim 40$  and  $\sim 0.02$  nA can be switched with a write and an erase gate voltage pulses of  $-6$  and  $+6$  V in a controllable manner, respectively. The measured on/off ratio were kept on  $\sim 10^3$  as the write/erase operations repeating. In right part of the figure, the retention test shows that both the on- and off-state of the memory can be well retained within a period of up to 1 week, after which the on/off ratio is still  $>10^2$ . (b) Test of nondestructively reading-out for more than two hundreds of times. The on/off ratio is keep on  $\sim 10^2$  and well separated from the drain current of the memory device before poling, which is defined as the reference current here.

**Table 1.** Memory Window  $\Delta V_{\text{th}}$  and Calculated Remnant Polarization Difference  $\Delta P_{\text{cal}} (= 2P_r)$  at  $V_G = 0$  V for CNT-FeFET Memory Devices with Wide Geometric Distributions Under Various Sweeping Gate Voltage Ranges

CNT-FeFETS	A	B	C	D	E
channel width ( $\mu\text{m}$ )	10	6	2	1	0.6
sweeping voltage (V)	$\pm 6$	$\pm 6$	$\pm 4$	$\pm 3$	$\pm 4$
$\Delta V_{\text{th}}$ (V)	5	4.5	3.5	4	4
$\Delta P_{\text{cal}}$ ( $\mu\text{C cm}^{-2}$ )	8	7	7.5	6	6.5

device again, and both the on- and off-state can be well retained. The record indicates a data retention time comparable to the state-of-the-art conventional FeFETs with its longest time of a month.<sup>18</sup> In fact, the small band gap of semiconductor SWCNTs ( $\sim 0.5$  eV) offers unique capability for stabilizing the remnant polarization of the ferroelectric films due to a suppression of the depolarization field during the memory retention interval.<sup>16,24</sup> The reading procedure can be repeated hundreds of times for both on- and off-states, respectively, as shown in Figure 2b. Since the negative or positive pulses induced a downward or upward remnant polarization state of the ferroelectric thin films, we have

retentively and nondestructively read the remnant polarization and thus the bistable states of the ferroelectric memory via reading the drain current.

In principle, if we assume that the polarization of the BaTiO<sub>3</sub> induces equivalent charges per unit area in the SWCNTs, the polarization difference of the BaTiO<sub>3</sub> between the “1” and “0” states at a given  $V_G$  can be calculated<sup>4</sup> by

$$\Delta P_{\text{cal}}^{V_G} = \Delta Q^{V_G} = \Delta I^{V_G} / \mu W E \quad (1)$$

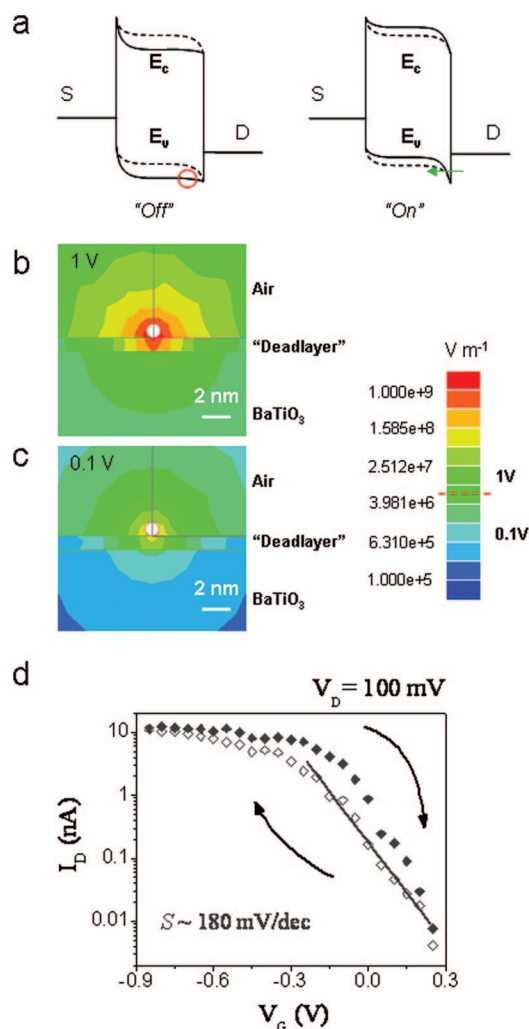
Here  $\Delta Q^{V_G}$  and  $\Delta I^{V_G}$  are the differences of the charges per unit area and the drain current in the tube between the “1” and “0” states at  $V_G$ , respectively.  $\mu$  is the effective mobility of the tube,  $E$  is the electric field along the conducting channel, and  $W$  is the diameter of the tube.

But this equivalence requires justification. In fact, the effective device width for a nanotube transistor should be larger than the nanotube diameter because the charge distribution spreads over a larger width than the tube diameter.

In order to shed light on the ferroelectric origin of the hysteresis observed in the  $I_D$ - $V_G$  transfer characteristics, we have tabled the memory window  $\Delta V_{\text{th}}$  of the hysteresis loops and the calculated remnant polarization difference  $\Delta P_{\text{cal}} (= 2P_r)$  at  $V_G = 0$  V for CNT-FeFET memory devices with a wide geometric distribution under various sweeping voltage ranges. The five devices are summarized in Table 1, showing that the  $\Delta V_{\text{th}}$  maintains  $3.5 \sim 5$  V at a moderate operation voltage of  $\pm 6 \sim \pm 3$  V with a SWCNT channel length of 10  $\mu\text{m}$ , 6  $\mu\text{m}$ , 2  $\mu\text{m}$ , 1  $\mu\text{m}$ , or 600 nm, respectively. The  $\Delta P_{\text{cal}}$  at  $V_G = 0$  V (determined from eq 1) exhibits the same trend as that of  $\Delta V_{\text{th}}$ , that is, maintains  $6 \sim 8 \mu\text{C cm}^{-2}$  regardless of the large variations of the sweeping gate voltage range and channel length. It is clear that although widely varying both the channel width and the sweeping gate voltage range, almost identical  $\Delta V_{\text{th}}$  and  $\Delta P_{\text{cal}}$  values are obtained, which closely resemble the typical behavior of the coercive voltage and the remnant polarization of a ferroelectric, respectively. Thus the calculations provide an unambiguous evidence for the ferroelectric nature of the observed  $I_D$ - $V_G$  clockwise hysteresis loop. These results open a way to tailor the memory hysteresis loop so as to control the memory switch of a CNT transistor memory, thereby meeting an important requirement for potential practical applications.

Figure 3a shows the operation principle of a CNT-FeFET (p-type). When a positive gate voltage pulse is applied between the SWCNT conductive channel and the metallic STON gate, the polarization in the ferroelectric film will be realigned toward the ferroelectric-SWCNT interface. After the gate voltage pulse is wiped out, the positive remnant polarization of the ferroelectric thin film will induce a downward band bending of the SWCNTs, corresponding to a thicker Schottky barrier. It will “cut off” the conductive channel of the p-type SWCNT FeFET,<sup>5</sup> representing a binary “0” state of the memory device. Reversely, when a negative gate voltage pulse is applied, a binary “1” state will be obtained. Thus a one-bit ferroelectric memory is demonstrated. The nonvolatile nature is ensured by the remnant polarization of the ferroelectric thin film, and the NDRO operation is fulfilled by reading the drain current of the FET.





**Figure 3.** (a) Operation principle of a CNT-FeFET memory. “Off” state: a positive gate voltage pulse induces a positive remnant polarization state in the ferroelectric film, resulting in a downward band bending of the SWCNTs, thus turn off the SWNT conductive channels. “On” state: a negative gate voltage pulse induces a negative remnant polarization state in the ferroelectric film, resulting in an upward band bending of the SWCNTs. As a result, holes are injected from the drain through tunneling, and the SWCNT conductive channels are turned on. (b–c) Calculated electric field mappings around the SWCNT channel at 1 and 0.1 V gate voltages, respectively. The red dashed line in scale bar indicates the measured coercive electric field of the ferroelectric film. (d) Transfer characteristics of the FeFET memory unit with a 300 nm SWCNT as conducting channel.

An important effect should be highlighted here, that is, the electric-field enhancement effect<sup>28</sup> originates from the ultrathin SWCNT. As shown in Figure 3b (poling with 1 V), the theoretical electric-field mapping reveals that much higher electric field ( $\sim 2 \times 10^7$  V m<sup>-1</sup>) could be reached near the contact between the SWCNT channel and the ferroelectric film, which exceeds the coercive electric field ( $\sim 6 \times 10^6$  V m<sup>-1</sup>) needed to polarize the ferroelectric film as indicating by the red dashed line in the color bar. The simulation indicates that the nanotube-based FeFET memory unit could be polarized (or written/erased) at a gate voltage ( $< 1$  V) much lower than the coercive voltage ( $\sim 2$  V) of the ferroelectric film. The simulation is consistent with our

experiments. As shown in Figure 3d, the CNT-FeFET memory exhibits memory loop at operation voltage less than 1 V with an impressing low subthreshold swing,  $S = dV_G/d \log(I_D)$ ,  $\sim 180$  mV per decade, which is comparable to that ( $\sim 70$ – $100$  mV per decade) of the state-of-the-art CNT-FETs. Therefore, it is clear that the memory can indeed be operated at low voltage less than 1 V, although with a compromised memory window. The simulation also indicates that a small reading drain voltage of  $\sim 0.1$  V, as shown in Figure 3c, used to discriminate memory states is not likely influence the polarization states of the memory, because the electric field ( $\sim 2 \times 10^6$  V m<sup>-1</sup>) that it causes is well beneath the coercive field of the ferroelectric film due to the existence of a so-called “deadlayer”,<sup>29,30</sup> which is an universal phenomena for ferroelectric films.

Usually, the width of the  $I_D$ – $V_G$  hysteresis loop of the CNT-FET exhibits a significant dependence on  $dV_G/dt$ , that is, the sweeping rate of the gate voltage due to the charge-storage effect.<sup>7–13</sup> In this study, the possible charge traps have been minimized and the charge-storage effect has been suppressed to a large extent by applying high-quality epitaxial ferroelectric films as gate dielectric, prebaking and measuring in dry air under relatively low gate voltage. Since we observe no width dependence of  $dV_G/dt$  in the hysteresis loops of the memory (see Supporting Information, Figure S3) and only clockwise  $I_D$ – $V_G$  hysteresis loops present in the present measurements, we conclude that the ferroelectric memory effect plays a dominant role over the charge-storage memory effect in the nanotube-based FeFETs.

In conclusion, our results constitute, to the best of our knowledge, the first experimental demonstration of the controllable switching, NDRO operation, and some of the most attractive performances of a CNT-FeFET memory unit, that is, data retention time longer than 1 week, large memory windows  $\sim 4$  V, and ultralow power consumption (energy per bit) of  $\sim$ femto-joule. Further simulations and experimental results show that the memory device is valid under operation voltage less than 1 V due to an electric-field enhancement effect induced by the ultrathin SWCNTs. Most importantly, the present CNT-FeFETs exhibit an intrinsic ferroelectric-dependent hysteresis memory loop thus a well-defined memory switch behavior, thereby meeting an important requirement for the potential practical applications.

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**Supporting Information Available:** Surface morphology and ferroelectric measurements of the ferroelectric films,  $dV_G/dt$ -independent hysteresis loops of the CNT-FETs, and a summary of the dielectric and electrical parameters of CNT-FeFETs with a wide geometric distribution under various sweeping voltage ranges. This material is available free of charge via the Internet at <http://pubs.acs.org>.

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